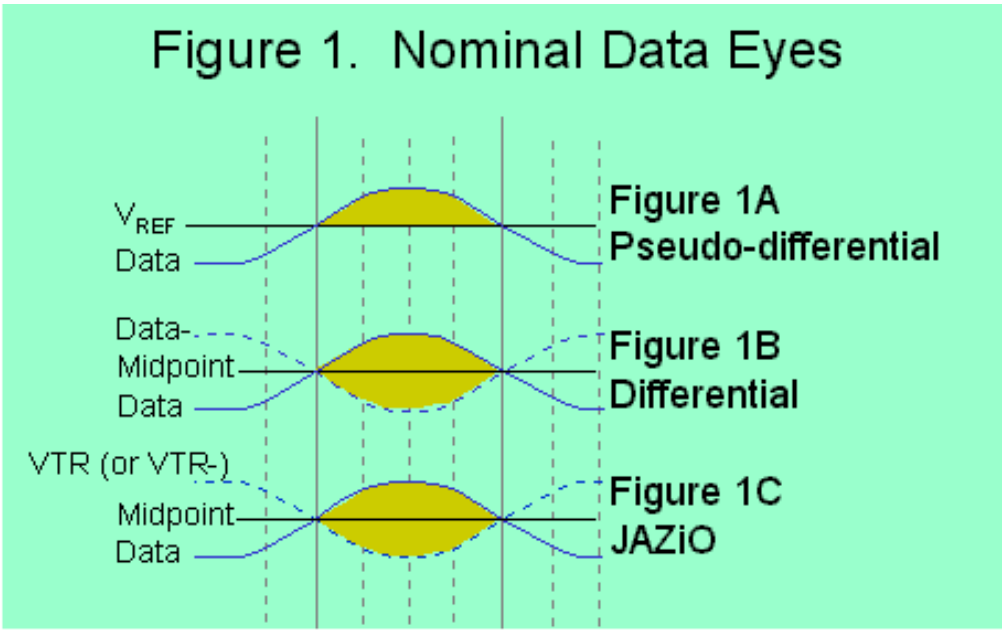
Improving Performance of Parallel Interfaces using Steady State Voltage and Timing References

I. INTRODUCTION

Until recently the choice for the digital signal switching technology used for parallel data transmission between integrated circuits was limited to either pseudo-differential technology with a single pin per data bit and a fixed VREF or differential technology with true and complement pins per data bit. JAZiO technology provides a third choice with a single pin per data bit and two Voltage/Timing Reference (VTR) signals instead of either fixed VREF or complement data pins. For a fundamental description of JAZiO technology see reference [1]. Figure 1 illustrates the data eyes for the three technologies for the nominal case with normalized voltage amplitudes. Signals are shown as approximately sine waves as is the likely case for high speed switching. This paper concentrates on positive going data pulses only for simplicity.

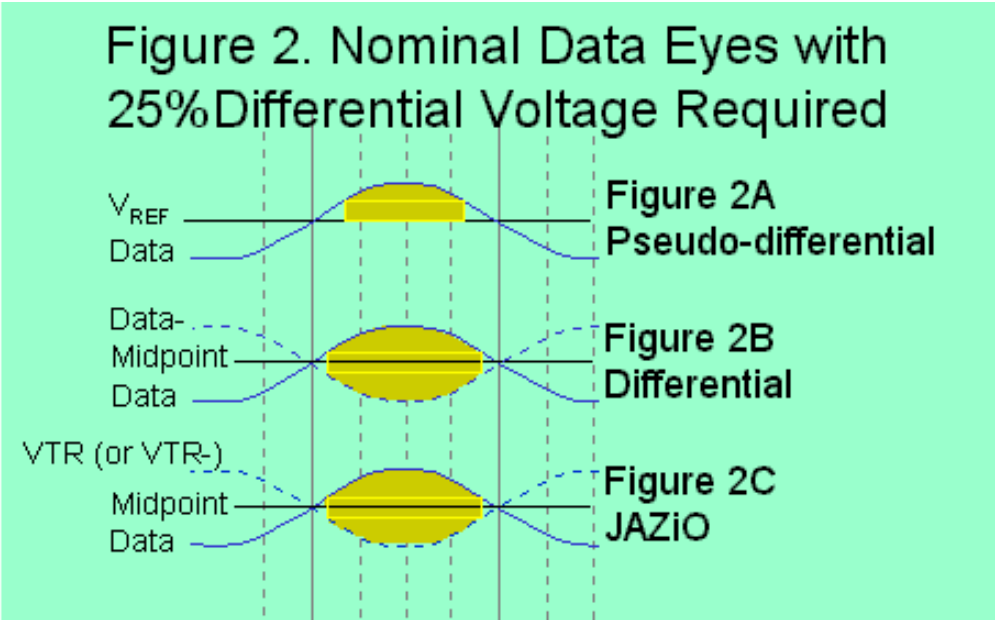


With a single pin per data bit, pseudo-differential has inherent cost advantages which helped establish it as the dominant technology used for parallel interfaces in the majority of integrated circuits, e.g., memory, microprocessor, controller, etc. Differential technology, with a complementary pair of signals per data bit, has certain advantages in both the receiver and the transmitter and has gained success in most serial interfaces and many parallel interfaces such as LVDS, HyperTransport, and RapidIO.

Data Eyes

A switching technology data eye can be defined as the voltage and time where a receiver can attempt to detect a data value. Since the pseudo-differential data eye (see figure 1A) does not begin to open until the data signal has crossed the VREF signal, usually at the midpoint voltage between data high and data low, and, from then on, the receiver differential voltage develops slowly since VREF is a fixed voltage. Hence, pseudo-differential, though cost effective, is slower than differential technology. The differential data eye (figure 1B) develops quickly because the data signal and its complement are moving in opposite directions. The JAZiO data eye also develops quickly because the data signal and the VTR signal (or VTR- signal) are also moving in opposite directions. Thus, JAZiO achieves one of the primary benefits of differential

technology without requiring two pins per data bit. Therefore JAZiO technology allows high performance at low cost.



The data eyes of figure 1 may be thought of as theoretical data eyes since an actual, real world receiver requires some finite differential voltage to be developed before it can sense the polarity of the input signal. If we assume that this required differential voltage is 25% of the total voltage amplitude of the source signal then we get the data eyes of figure 2. As the data rate increases the corresponding bit time is proportionately reduced. The width of the data eye depicts the time available to latch the signal. The height of the yellow box is 25% of the total voltage swing. The width of the yellow box as defined by the intersection of the data eye and the minimum required signal is of primary importance. As the data rate increases this width decreases. Notice how the pseudo-differential data eye in figure 2A is much reduced from that in figure 1A while the data eyes for the other two technologies are not so greatly reduced from figure 1 to figure 2. This effect clearly illustrates the effectiveness of differential sensing used in differential and JAZiO technologies.

The following discussion examines non-nominal cases such as bit-to-bit skew, ISI/attenuation, and signal pushout due to crosstalk, SSO, etc. and explains how steady state VTRs improve the performance of JAZiO technology in parallel interfaces.

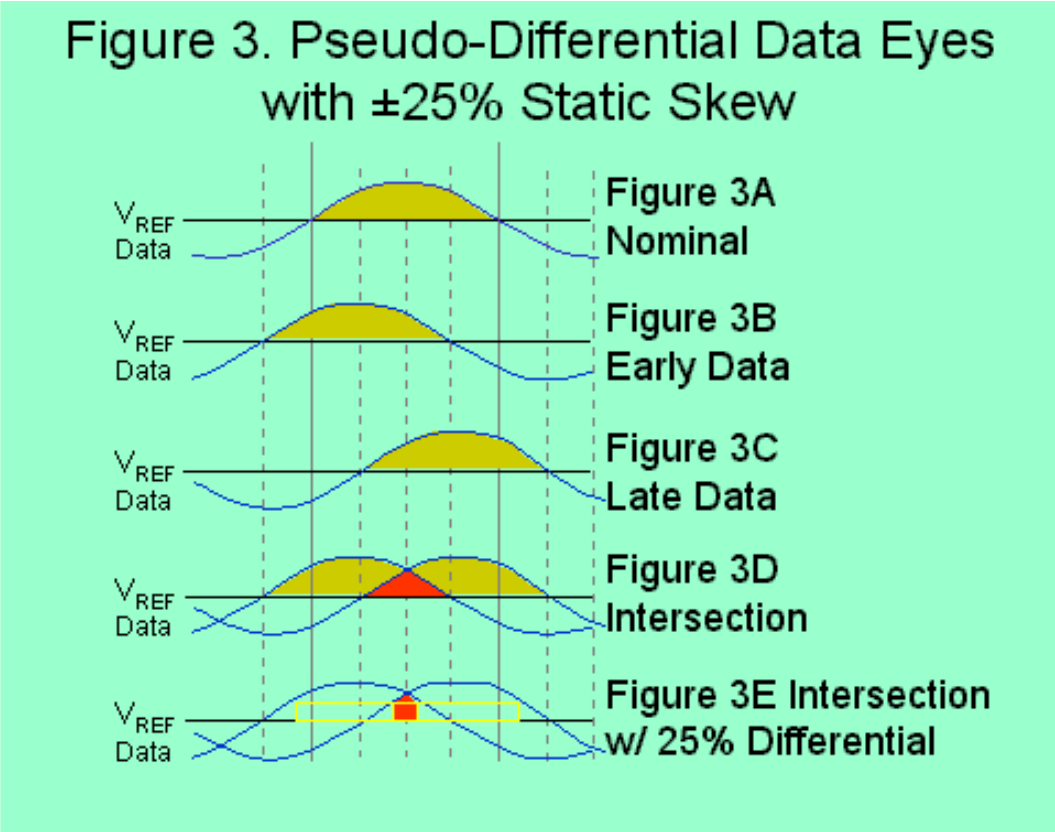
II. Bit-to-Bit Skew

Bit-to-bit skew is the difference in the arrival times of the various bits of a parallel interface at their respective receivers. This skew can be divided into static skew and dynamic skew. The static skew for a given interface is dependent on mismatches in pre-driver, driver, package, PCB, routing to the receiver, etc. The dynamic skew is related to simultaneous switching outputs (SSO), crosstalk between the bits, reflections, etc. The eye diagram with the effect of bit-to-bit skew is explained for identically transmitted signals for pseudo-differential, differential and JAZiO receivers. The amount of skew considered here is 25% of the bit time in both directions.

Pseudo-differential skew

Figure 3 illustrates pseudo-differential data eyes with an early data bit (figure 3B) that arrives 25% of a bit time earlier than the nominal (no skew) case and a late data bit (figure 3C) that arrives 25% later than nominal. Notice that the data eyes for the skewed data are the same shape as the data eye for the nominal

data but are moved in time by 25% of a bit time. Figure 3D shows the intersection of the nominal, early, and late data eyes in red. Figure 3E shows this intersection with a required differential of 25% of the total voltage swing. Notice how this intersection is very small. When receiving parallel data, the receiving chip must amplify or level convert each bit separately and then assemble the various bits into a parallel word and a very small intersection makes the assembly extremely difficult.



Differential skew

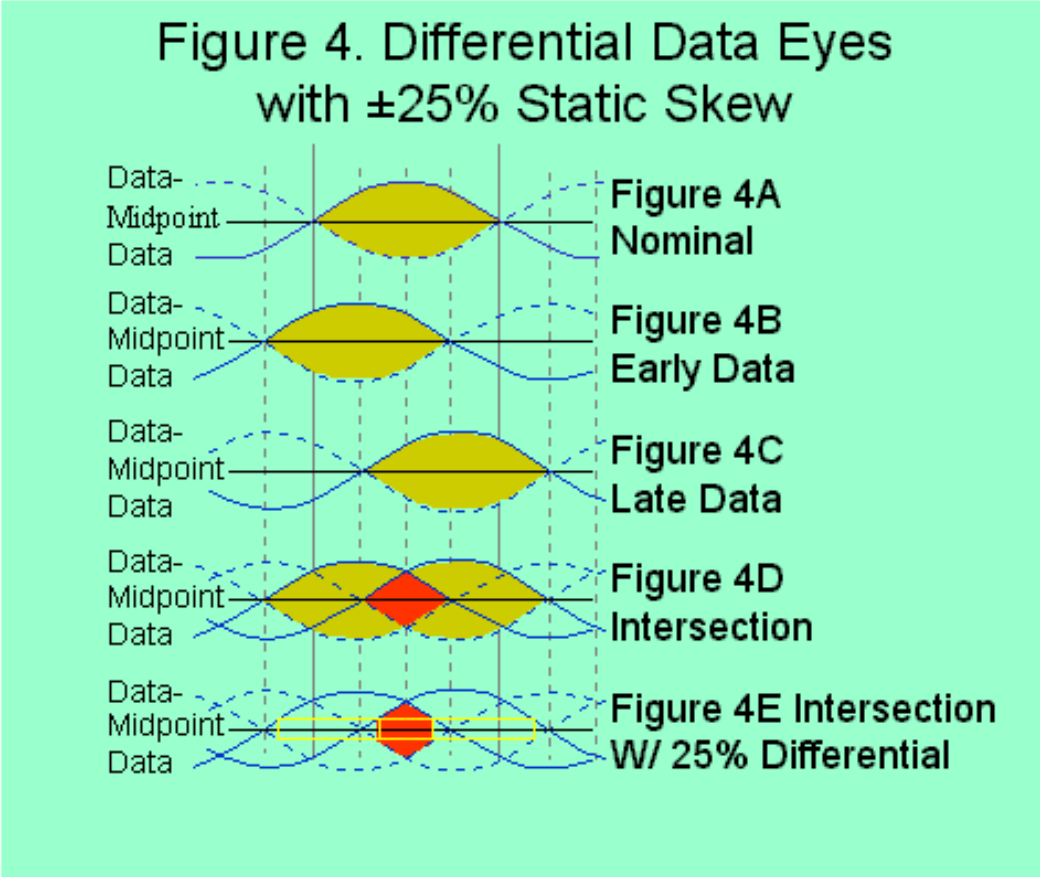
Figure 4 illustrates the same effect for differential technology. Notice that, again, the data eye does not change shape due to skew but the intersection of the early data eye and the late data eye is small. Figure 4E shows this intersection with a required differential of 25% of the total voltage swing. This intersection is reduced from that of figure 4D but does not have as large a reduction as the reduction for pseudo-differential technology.

JAZiO skew

Figure 5 illustrates this effect for JAZiO technology. In this case, notice that the data eyes for the skewed data do change shape. The reasons for this are (1) JAZiO data eyes begin and end when the VTR signal (or VTR-) across the data signal rather than when the data signal crosses the midpoint voltage and (2) the VTR (or VTR-) signal does not move with skew since the same VTR signal is used in all the receivers. Also, notice that the data eyes for the skewed data are larger that the corresponding data eyes for skewed data for pseudo-differential and differential technologies. Notice, too, that the intersection (figure 5D) is larger than the intersections for the other two technologies being about ¾ of a bit time wide rather than ½ bit time. The reduction in intersection height is also less than for the other two technologies. Finally, notice that in figure 5E the intersection with 25% differential voltage is reduced by only a small amount. For these reasons JAZiO technology has more inherent skew immunity than do the other two technologies and can operate at higher data rates with the same skew.

Limitation due to skew

Skew of 25% of a bit time in both directions from nominal is chosen here to illustrate the concept that JAZiO technology, by use of common voltage and timing references, is more immune to static skew than are the other two technologies. In an actual system static skew can be much larger than ±25%. Static skew is mostly caused by manufacturing tolerances and, therefore, is difficult to accurately measure until the devices are mounted on a board. Static skew does not scale with increasing data rate. Therefore, as data rate is increased, each of the three technologies will reach some data rate at which it is limited by static skew. At that point either manufacturing tolerances have to be improved or some deskewing technique has to be employed.



Differential and pseudo-differential technologies do not have an easy technique to determine the static skew between different bits of a parallel interface. In parallel interfaces, both pseudo-differential and differential technologies have a voltage reference that is separate from their timing reference. The voltage reference, VREF for pseudo-differential or the complimentary signal for differential, is used for level conversion only. The timing reference, usually a differential clock or strobe provided to latch the data after level conversion, is usually transmitted with a 90-degree phase shift. Therefore, there is no timing signal aligned with the parallel data transfer that can be used to determine the skew during operation.

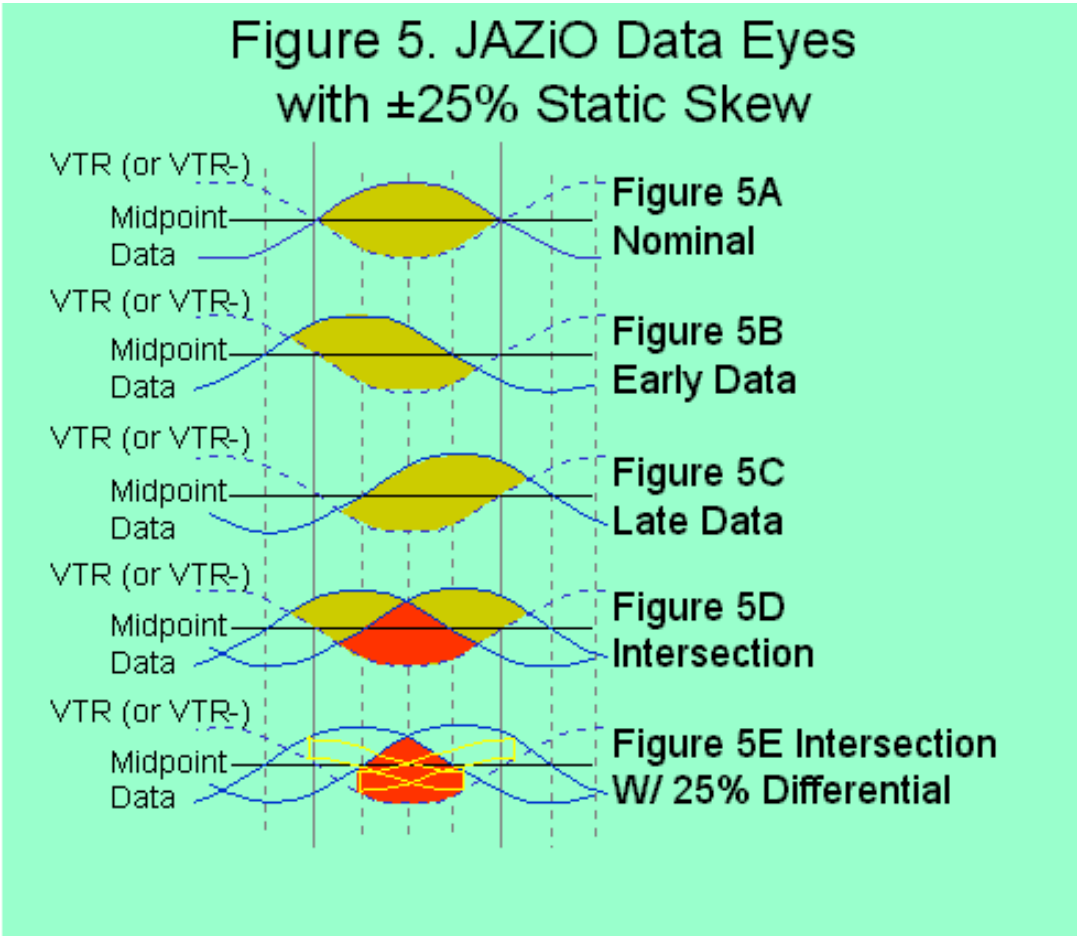
Deskewing static skew

One deskew method is to use tuning cycles to adjust a programmable delay on either the driver or the receiver latch and record the pass/fail result of each receiver at each delay. Before actual operation begins the programmable delay is set to the center of the “pass” window. A difficulty with this method is that at high data rates the granularity of the programmable delay is large relative to the bit time and, therefore, the “pass” window is small in terms of the delay granularity. Thus, it is difficult to truly center the programmable delay

and it may, in fact, be set to a value very near to the edge of the "pass" window and a small drift during operation may cause failure.

JAZiO Receiver Monitor

JAZiO technology provides an enhanced method of deskew. See reference [2] for a description of the JAZiO receiver monitor which provides a signal indicating that the receiver is operating properly but is near the point where skew will cause failure. Combining this receiver monitor with the above deskew method provides an envelop around the "pass" window that allows programmable delays to be set at values that are not close to failure. Therefore certain drift during operation can be tolerated and, in fact, in "long uptime" products the receiver monitor can be used during operation to signal that a tweak to a driver delay should be made before any failure occurs.



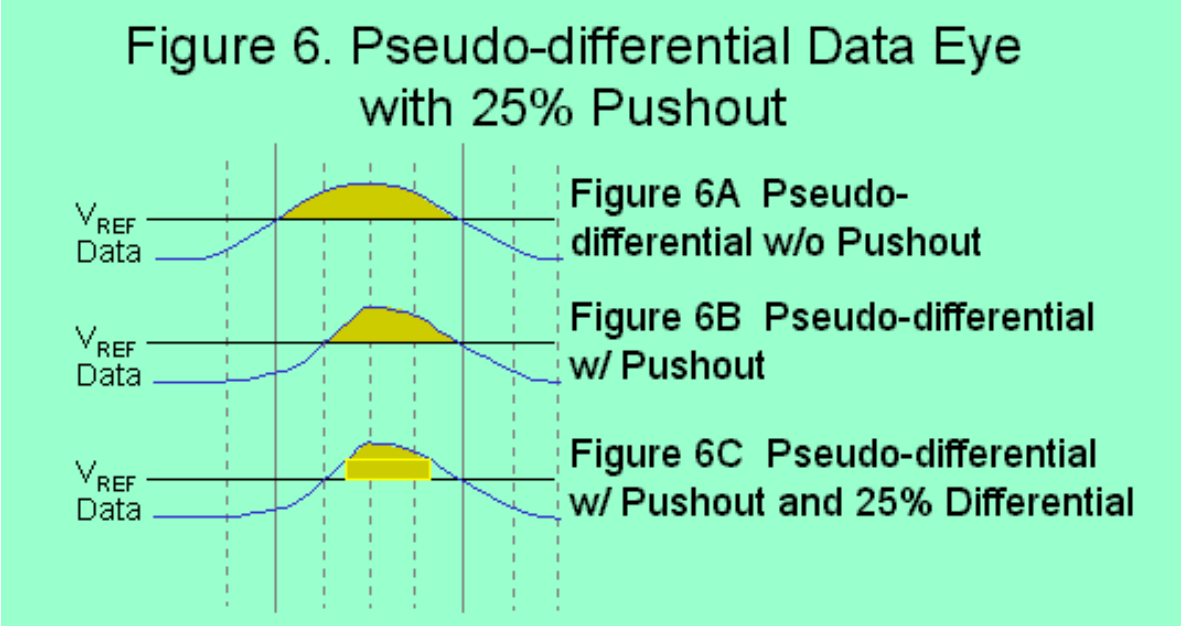
Conclusion on Static Skew

Due to the common voltage and timing references of JAZiO technology it is inherently more immune to static skew than the other two technologies and can operate at higher data rates with the same skew. Due to the JAZiO receiver monitor, JAZiO technology allows an accurate method of in-system deskewing that allows even higher data rates.

Dynamic Skew (pushout)

A single-ended signal can be significantly affected by adjacent bits due to crosstalk or the effect on supply voltages due to simultaneous switching outputs (SSO) in high inductance wire bond packages or connectors. Here we refer to the effect of crosstalk and SSO as pushout of a signal as it is delayed from the nominal case. Pushout is reduced in differential signaling if each signal and its complement have negligible skew. The effect of pushout totaling 25% of a bit time in the case of pseudo-differential technology is shown in

figure 6B. The width of the data eye is directly shortened by 25%. Figure 6C shows the data eye with a required differential of 25% of the total voltage swing resulting in a very small eye.



The same 25% pushout in the case of JAZiO is shown in Figure 7B. The effect is significantly less in JAZiO, as the corresponding VTR is not affected in time or amplitude. Figure 7C shows the data eye with the 25% differential requirement. Notice the small reduction in eye from figure 7A to 7B and from 7B to 7C.

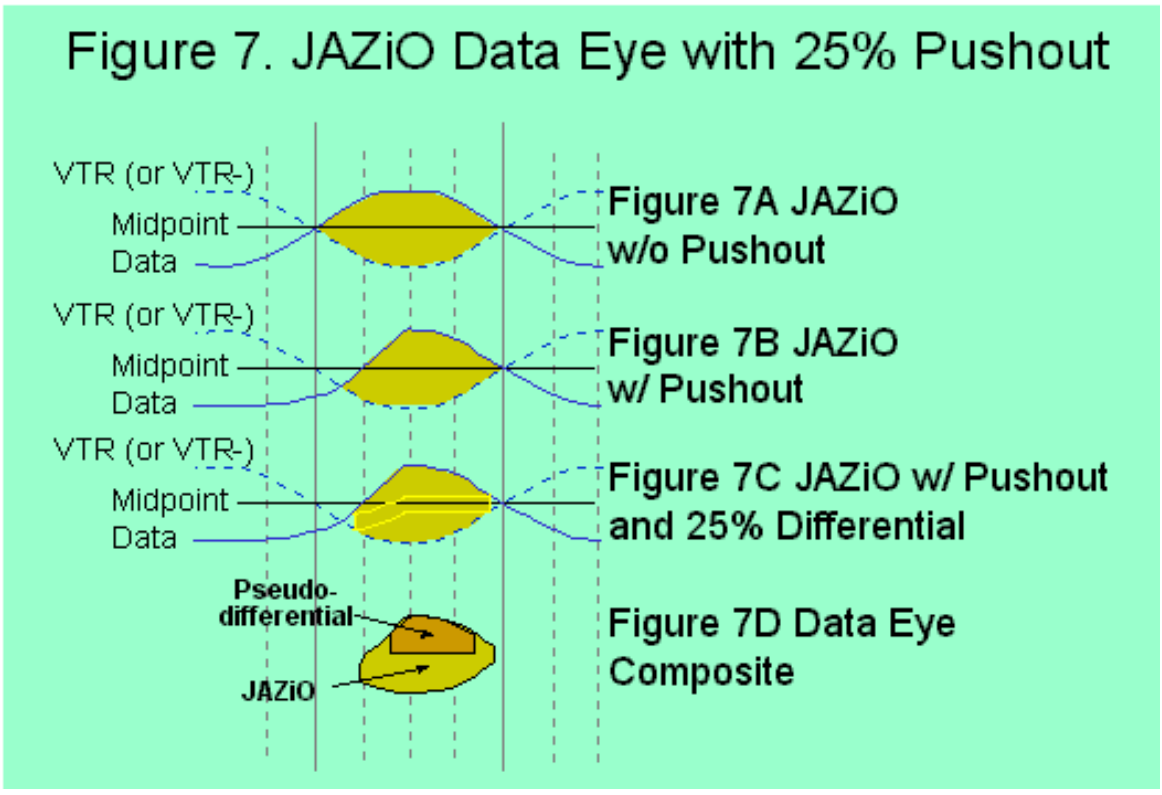
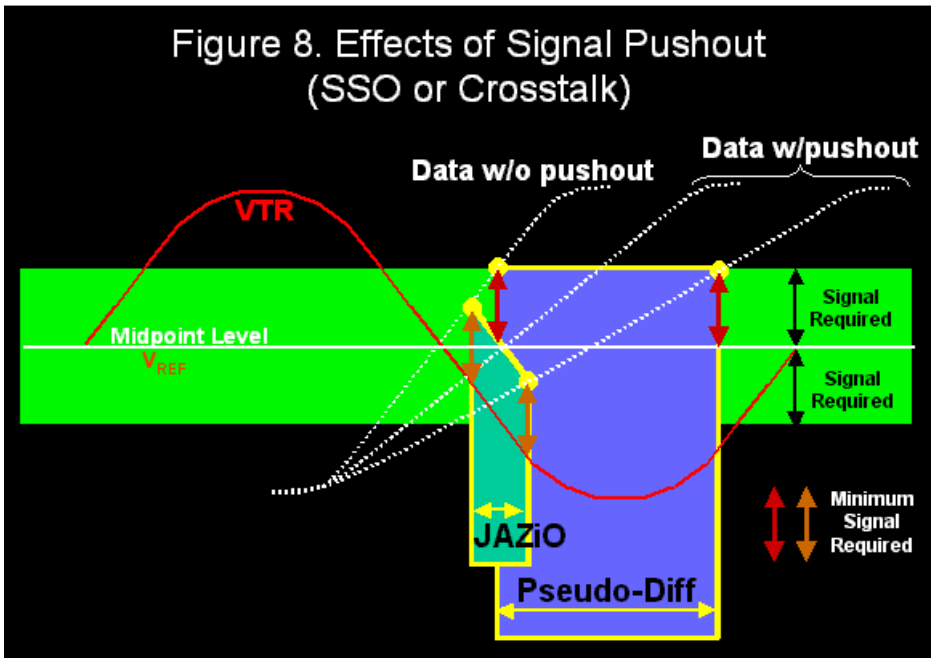


Figure 7D is a composite showing the data eyes with 25% differential from figure 6C and figure 7C on top of each other in order to illustrate the large data eye size advantage for JAZiO technology compared to pseudo-differential technology with 25% pushout. Figure 8 shows this in more detail where the signal exhibiting the push out has a slower transition time than the nominal signal. Since the VREF level is fixed in Pseudo-differential, the signal crosses VREF latter in time. The required signal amplitude for the receiver to amplify the voltage difference further effects the timing variation from the nominal case. The VTR in JAZiO cases remains unaffected, therefore the crossing of the signal (push out with SSO and crosstalk) and VTR occurs below the midpoint (similar to static skew case). Also the required signal is developed faster as the VTR is transitioning at the nominal rate. The overall effect of pushout is about 4 times less with JAZiO than with Pseudo-differential.



Voltage amplitude

Due to the small data eye of pseudo-differential technology it is normal practice to operate it with larger voltage amplitudes. However, larger amplitudes result in more dynamic skew (as well as more power) by causing more SSO and more crosstalk. Therefore, larger amplitudes are not a satisfactory solution to pushout in pseudo-differential technology. JAZiO technology, with its large data eye, does not need large voltage amplitude and can be used with the lower amplitudes commonly used for differential technology.

Single-ended driving

Differential technology is noteworthy for having reduced dynamic skew. This reduction is primarily due to the equal number of signals switching in opposite directions, thus reducing SSO. It is also common practice to route a differential signal pair very close to each other compared to the distance to other pairs, thus reducing crosstalk to other signals. Since differential technology is clearly superior to pseudo-differential technology in regard to dynamic skew, there is the question of: "Can single-ended driving be used in high performance switching?"

JAZiO technology, with its large data eye effectively uses single-ended driving at very high data rates. Generally speaking, a low inductance package like flip-chip or chip scale BGA causes little pushout due to SSO in single-ended transmission. If very large numbers of drivers are needed on a single chip then data encoding with balanced codes in the horizontal dimension can reduce the effect of SSO and crosstalk in

single ended transmission. The effect of SSO can be reduced on the VTR signals by using a separate power supply or a power supply isolated from the single ended drivers and by incorporating differential termination between the complimentary VTR signals. Crosstalk can be reduced by providing a power or ground plane close to the signals on the board for signal return path and separating the signals equidistance from each other resulting in the same overall pitch as differential routing. The effect of crosstalk can be further reduced on VTRs by isolating them from other signals by power or ground lines. Note that the effects of crosstalk and SSO are not additive as SSO pushes out the majority of the signals moving in the same direction, whereas crosstalk pushes out one signal moving in one direction surrounded by the other signals moving in the opposite direction.

It should also be pointed out that the typical method for routing differential signals, with tight spacing inside pairs and large spaces to other pairs, results in pushout of differential signals. Since this pushout is always predictable it is not considered noise. However, since the signals of a pair are coupling negatively onto each other, they slow the overall transition times required to switch signals. At very high data rates this pushout can limit performance. The seriousness of this effect is easier to visualize when it is remembered that, in order to match performance per pin, differential signals must switch twice as fast as single-ended signals.

Conclusion for bit-to-bit skew

In conclusion JAZiO receivers are inherently more immune to bit-to-bit skew than differential or pseudo-differential receivers for identically driven signals. By comparing the size of the eye diagrams of the three technologies, we can infer the size of the eye related to each of the signals or reference. The eye size of Pseudo-differential is exactly half that of differential. Therefore each complimentary signal of the differential switching technique contributes half of the total eye size. The eye size in the JAZiO case is larger than the differential case, which is attributable to the same VTR acting as a complimentary signal to both data signals. Therefore the eye size contribution of VTR is more than half of the total eye size.

III. ISI/Attenuation:

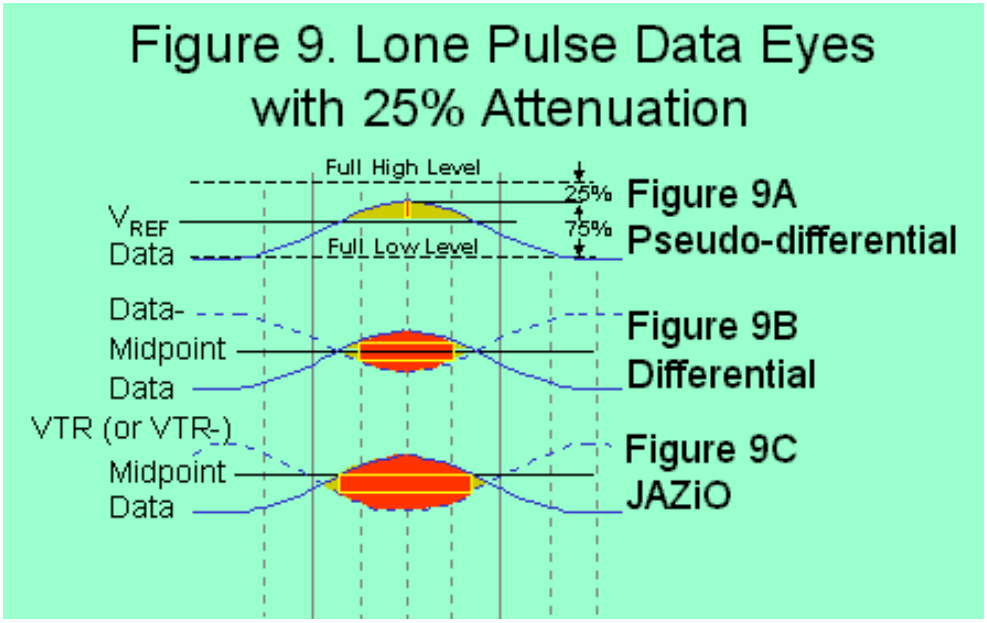
ISI (Inter-symbol Interference) is the data dependent noise on a signal in one bit time due to data values on the same signal in other bit times. As the frequency and/or distances increase, transmission lines cannot be charged or discharged completely in a single bit time and signal attenuation and ISI occur.

Signal attenuation

For high frequency signals the voltage swing at the receiver is smaller than the swing at the transmitter due to signal attenuation. Even if the signal at the transmitter is driven like a square wave the signal at the receiver will approximate a sine wave because the high frequency components of the square wave are attenuated due to the lossiness of the PCB trace. A lone pulse is the worst case since the signal at the receiver has enough time to settle to the maximum high or low level of the transmitter before the lone pulse occurs. The leading edge of a lone pulse must start from the maximum signal level and, at high data rates, the bit time ends before the signal transition is complete at the receiver.

The eye diagram for the three technologies with the effect of ISI/Attenuation is illustrated in figure 9 for identically transmitted signals. Signal attenuation of 25% is used in this report and this is a reasonable assumption for signal rates of 2Gbits/sec with FR4 PCB.

Notice that for pseudo-differential and differential technologies the resulting data eyes are much reduced from the nominal eyes in figure 1 being only ½ the height and about 3/4 the width. The reduction in height is due to attenuation and the reduction in width is known as ISI jitter. When applying the requirement of a differential sensing voltage equal to 25% of the total voltage amplitude (shown by the yellow boxes) we get the resulting red data eyes. Notice that for pseudo-differential technology the total height of the data eye is only 25% of the signal swing so there is no red eye. This effect clearly illustrates why pseudo-differential technology must employ larger voltage amplitudes.



The JAZiO data eye shown in figure 9C is larger than the other two. The reason for this is that the VTR signal is a continuous pulse changing every bit time and, therefore, suffers from attenuation but not ISI jitter. In addition its voltage waveform is centered around the midpoint voltage rather than starting its transition from the full high or low voltage level. Therefore, even though the peak-to-peak voltage of the VTR signal is attenuated, it still reaches a larger transition from the midpoint voltage than does a lone pulse data signal that is not centered. Therefore the JAZiO data eye is taller than the data eyes for the other two technologies. Also, as always, the JAZiO data eye begins and ends when VTR crosses the data signal. This "crossing" effect results in a wider JAZiO data eye just as has been shown for bit-to-bit skew and pushout.

Careful examination of figure 9 reveals that the "high" side of the data eye for each technology is formed by the data signal but the "low" side of each eye is formed differently. For pseudo-differential and differential technologies the low side is formed by VREF and data-, respectively, and those signals in no way alleviate the effect of ISI/attenuation that occurs on the high side. For JAZiO technology the low side of the eye is formed by the steady state, continuous VTR signal that "suffers less" from ISI/attenuation and helps to form a better eye. By looking at the low side of each data eye it can be observed that VREF provides 0% of the height of the pseudo-differential data eye and the data compliment provides 50% of the height of the differential data eye. For JAZiO technology the data signal provides about 37% and VTR provides about 63% of the height of the data eye for these conditions. Thus the VTR signal provides about 70% more height of the data eye than the data signal provides. Correspondingly the width of the yellow box for the differential case in figure 9B is 50% of the original bit time, whereas for the JAZiO case it is about 75% of the original bit time. Thus VTR provides 50% additional timing margin to latch the amplified signal as compared to the differential case.

Again it can be seen that when applying the 25% differential requirement the effect on differential and JAZiO technologies is far smaller than the effect on pseudo-differential technology.

Pre-emphasis

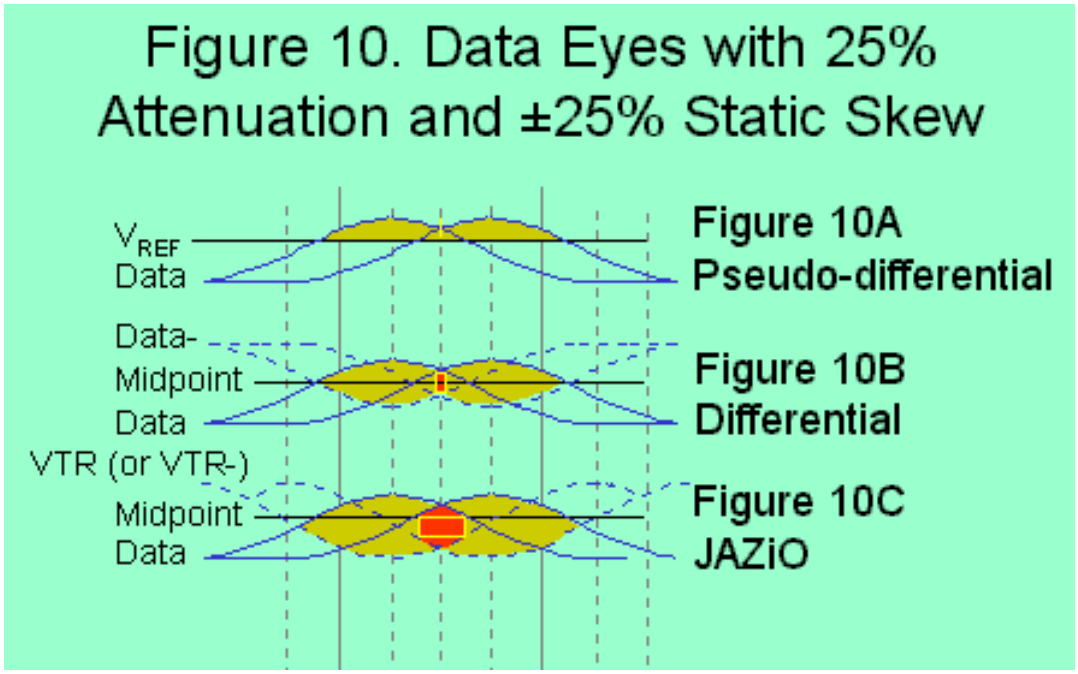
Pre-emphasis is a method sometimes used to reduce the effect of ISI/attenuation. The amount of voltage attenuation remains the same but the transition is made to begin at different voltage levels in order to reduce ISI jitter. Pre-emphasis can be used effectively for predetermined frequency and distance between transmitter and receiver in a point-to-point configuration and can be used with any of the three switching technologies including JAZiO. However, complexity increases as the frequency and distance become

variable. General purpose devices like memory, FPGAs, Chipsets, Controllers, etc. lose their flexibility of being used for various applications or have to operate with some amount of ISI jitter even with programmable pre-emphasis. Pre-emphasis may actually be impractical for multi-drop buses like memory since the distance to the receiver is different for each device. But in situations where the use of pre-emphasis is practical it can increase the performance of JAZiO technology just as much as any other technology.

Conclusion on ISI/attenuation

In conclusion JAZiO technology is inherently more immune to signal attenuation and ISI jitter than pseudo-differential or differential technology for identically driven signals. The reason for this is that JAZiO uses a steady state, continuous, voltage-centered VTR signal in its data eye and this VTR signal is less affected by ISI/attenuation. Therefore, JAZiO is especially well suited for general-purpose parallel interfaces which operate at different frequencies or variable distances or multi-drop buses since, in these cases, pre-emphasis becomes complex or impractical.

IV. Composite Eyes of Parallel Interfaces



In a real world product it is likely that static skew and ISI/attenuation, although having different causes, will both appear. Therefore the combined effect of them is now examined. Figure 10 shows the affect on data eyes of the technologies when ±25% static skew and 25% attenuation occur. Figure 10A shows two bit positions of a parallel transmission using pseudo-differential technology with each bit suffering from 25% signal attenuation and one bit being advanced by 25% of a bit time and the other being delayed by 25% of a bit time. In order for the receiving chip to assemble the bits into a parallel internal bus it is useful to have some common overlap in time when both bits can be sensed. It is also useful to have some reasonable differential sensing voltage (here assumed to be 25% of voltage amplitude at the source) during this overlap period. The yellow box indicates the 25% differential and the red data eye indicates the common overlap period when the 25% differential is achieved.

Notice that pseudo-differential technology does not come close to having any red data eye. Differential technology does have a small red data eye and it is possible that with enough clever engineering a differential system might be made to work with the assumptions used here. But JAZiO technology has a

reasonably large red data eye indicating that a system with JAZiO technology could be designed in a very straightforward manner without difficulty. JAZiO is the clear winner when static skew and ISI/attenuation are taken into consideration. Dynamic skew in the JAZiO case is considerably smaller than for Pseudo-differential. With appropriate power to signal pin ratio, package and PCB spacing, the JAZiO advantage of static skew and ISI/attenuation far outweighs the differential signaling advantage for dynamic skew in an overwhelming majority of parallel interfaces. Remember that the differential technology uses twice as many pins as JAZiO requires in all the comparisons made here.

V. RESULTS

Up to this point all comparisons have been made based on data eyes at receiver inputs. In this section simulation results and measured data are used to show the effects at receiver outputs. Figures 11 and 12 demonstrate the effect of attenuation and ISI using a 300bit PRBS pattern. These simulations are based on a 0.18u high performance CMOS process, Flip-chip package, and a 24-inch PCB trace using FR4. The 1.8V I/O voltage (figure 11 and 12) is necessary for backplane type applications to overcome signal attenuation.

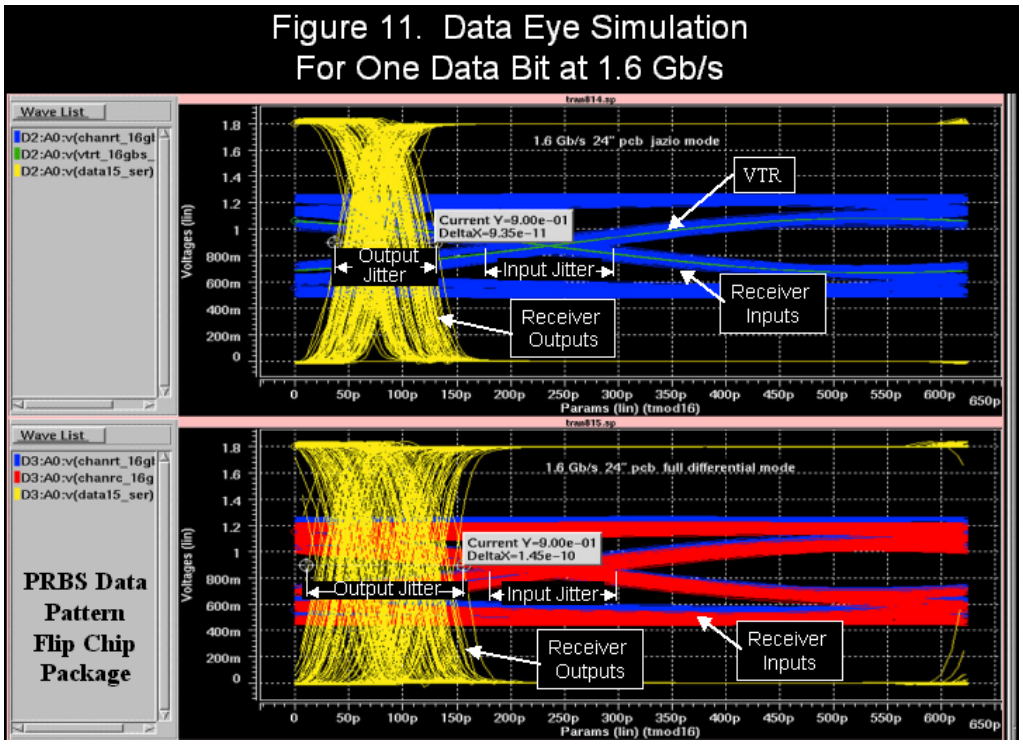
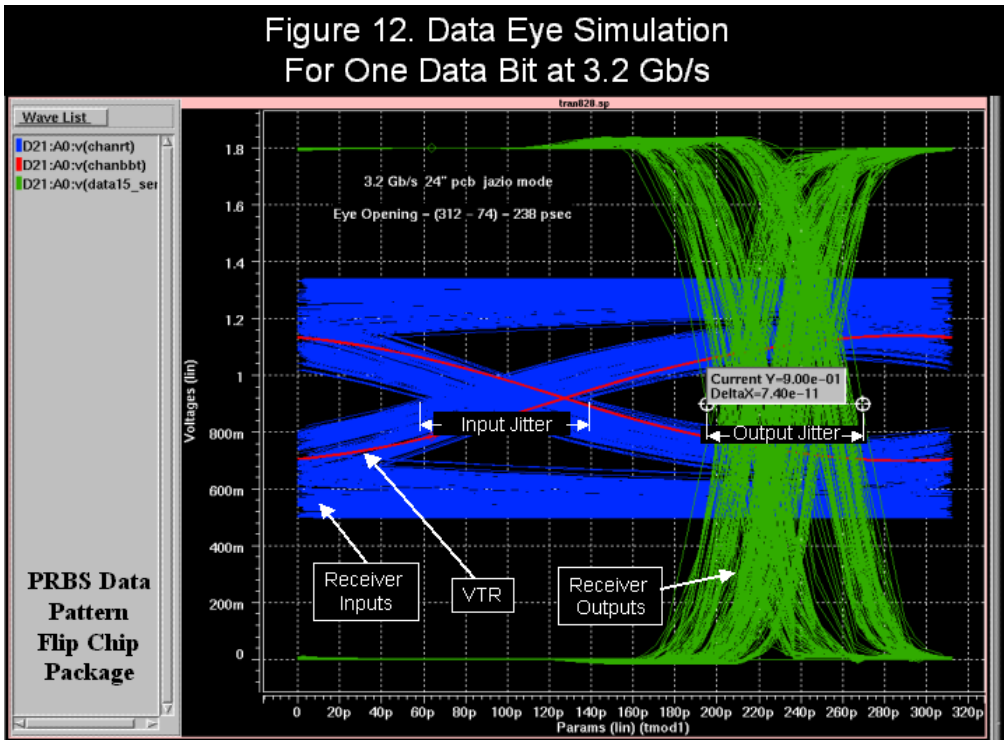
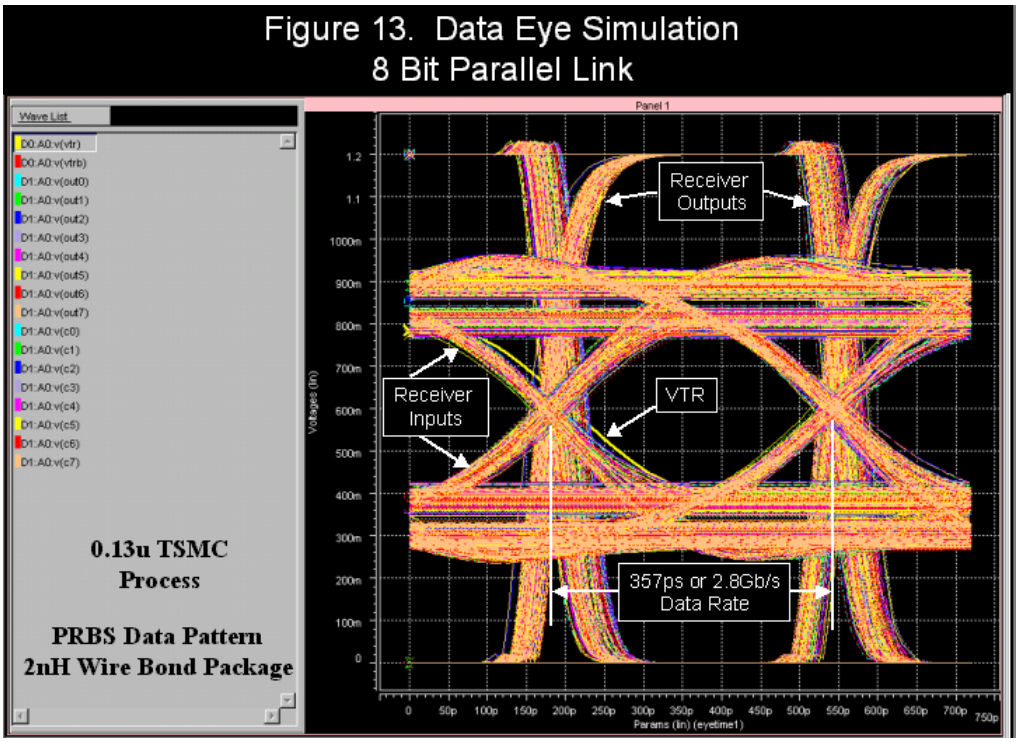


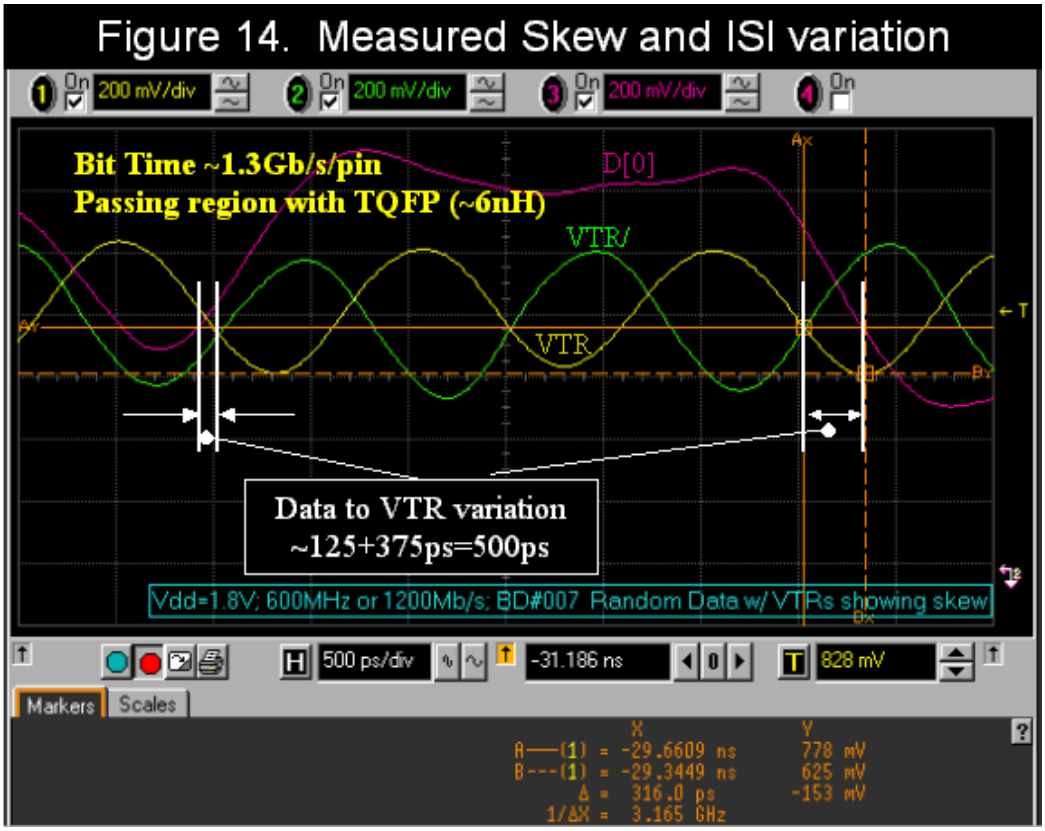
Figure 11 shows the comparison between JAZiO (top half) and differential (bottom half) at 1.6 gigabits/sec. The input data at the receiver inputs for both technologies has 115 pS of jitter. Output jitter for the JAZiO case is 93.5 pS and for the differential case is 145 pS. Since the bit time at 1.6 gigabits/sec is 667 pS it follows that the JAZiO receiver provides a stable output for 86% of the bit time while the differential receiver provides a stable output for 78% of the bit time. These results show that the JAZiO receiver provides a larger window of stable data at its output than does a differential receiver when the two receivers have identical inputs.

Figure 12 shows a JAZiO simulation at 3.2 gigabits/sec under the same conditions. In this case the input jitter is 80 pS and the jitter at the output of the JAZiO receiver is 74 pS, which is 76% of the 312.5 pS bit time. It should be noted that this simulation is demonstrating JAZiO operation at 3.2 Gb/sec/pin, which is a “per pin” bandwidth equal to differential technology at 6.4 Gb/sec/pair.



The effect of bit-to-bit skew in an 8-bit interface is shown in another simulation using a low power 0.13u CMOS process with a 9-inch PCB trace and a BGA wirebond package. The I/O voltage 1.2V is used to demonstrate low power applications (i.e. Memories). Figure 13 shows the composite of input signals for a 150-bit PRBS pattern and output signals for the 8 receivers. The pattern stresses various effects such as SSO, crosstalk, and bit to bit skew. Operation is at 2.8Gb/s per pin.





Results of a test vehicle to demonstrate the usefulness of JAZiO in a low cost environment is shown in figure 14. It is fabricated using standard cell libraries and 0.18u CMOS Foundry process. The package used is a standard TQFP with 4-6nH lead variation (center to corner). The PCB is FR4 with a 9" trace length. The figure shows the continuous VTR/VTR- relative to the worst case data bit (farthest away from VTR). The data leads VTR by ~125pS at the trailing edge of the lone pulse and lags VTR by ~375pS at the leading edge of the next lone pulse. The total variation of 500pS is approximately 65% of the bit time. The test chip has 16 parallel bits transmitted with a single VTR pair and is running a PRBS pattern of 2^{33-1} and passes above 1.3Gbs data rate. This demonstrates the robustness of JAZiO single ended signaling in the presence of skew for a parallel interface.

JAZiO vs differential technology

At high data rates the timing margins due to bit-to-bit skew and ISI/attenuation are the major limiters. The JAZiO receiver significantly improves timing margin in the presence of bit-to-bit skew and ISI compared to the differential receiver. If the dynamic bit-to-bit skew is less than the static bit-to-bit skew and ISI/attenuation, then single ended transmission with the JAZiO receiver is faster than differential transmission with differential receivers and has over twice the "per pin" bandwidth.

Differential transmission (driver and transmission channel) is superior to single-ended transmission for dynamic skew. But the differential receivers in the parallel interface do not have the means of reducing bit-to-bit skew or the effect of ISI/attenuation. The VTRs in the JAZiO receiver are better suited as references for the whole parallel interface than individual complimentary references for each signal in the differential receiver. Differential transmission combined with JAZiO receivers (using one signal from the differential pair and ignoring the compliment) provides the fastest and most robust parallel interface in the presence of bit-to-bit skew (both static and dynamic) and ISI/attenuation.

VI. Conclusion

In conclusion, the complimentary VTR and VTR- pair significantly enhances the data eye at the receivers of a parallel interface compared to VREF in Pseudo-differential technology or the complimentary signals of differential technology. In fact, VREF in Pseudo-differential does not contribute any signal amplitude or increase of the timing window in the presence of bit-to-bit skew or ISI/attenuation. Therefore, the Pseudo-differential receiver sees the full effect of attenuation on the signal amplitude and timing window reduction due to skew.

Each signal of the complimentary pair of differential technology provides half of the height of the data eye in the presence of attenuation as both the data signal and its compliment are attenuated equally. Each compliment has the same timing as the true data signal. Therefore differential receivers see the full effect of data eye intersection reduction due to bit-to-bit skew.

The complimentary VTRs contribution to the data eye height increases from 50% to 70% or more with an increase in attenuation. Correspondingly the VTRs also increase the data eye width by 50% or more with an increase in ISI or bit to bit skew. The VTRs, by being continuous, provide the best reference signal for a receiver. Since the VTRs are used as complimentary references for all the parallel signals, the effect of skew between the signals seen by their respective JAZiO receivers is reduced. As the signal rate increases without proportional scaling of bit-to-bit skew, ISI jitter, and signal attenuation, the VTR contribution stands out both in signal amplitude and timing margin. Thus, JAZiO technology is the best option for parallel chip-to-chip interfaces.

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