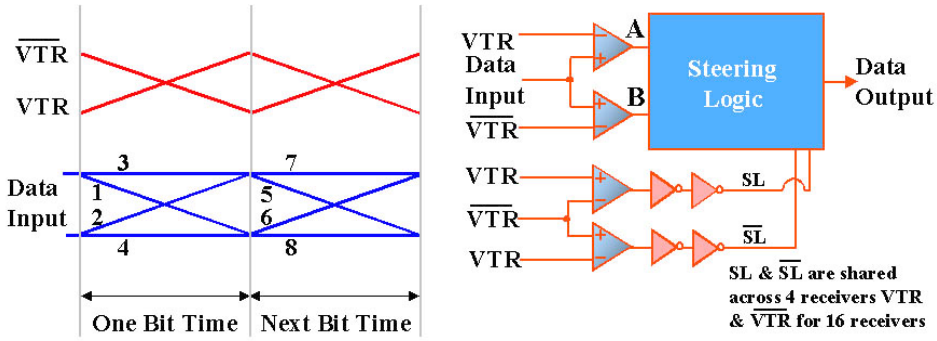
JAZiO SIGNAL SWITCHING TECHNOLOGY FOR LOW COST AND HIGH SPEED DIGITAL APPLICATIONS

INTRODUCTION: JAZiO is a digital signal switching technique, which uses differential sensing but requires only a single pin per signal. It is based on detecting change or no-change in the data signal from the previous state using a pair of alternating voltage and timing references (VTRs). A novel alignment monitoring scheme further enhances JAZiO capability for deskewing data signals and high speed testing of the interface. JAZiO is suitable for low latency, high-bandwidth applications like DRAMs (Memory Bus), SRAMs (Back Side Bus), CPUs (Front Side Bus), Network Processors, ASICs, SOCs (Intra-Chip buses) etc.



A) Data and Voltage Timing References (VTRs) **B)** JAZiO Receiver Block Diagram

Figure 1: Basic JAZiO elements

OPERATION: The JAZiO transmitter drives a pair of alternating voltage and timing references (VTRs) coincidentally with about 16 data signals onto a bus or a receiver in a point-to-point system. The VTRs are complements of each other (VTR and /VTR) as shown in Fig. 1A. The signal swing is 0.5V or less and the transition time can be as much as a full bit time to reduce the ground bounce, cross-talk, coupling, EMI, ringing etc. The VTR swing is about the same or less than the signals (depending on the data rate). The VTRs transition every bit time in which the signals are transferred. The output driver is standard impedance matched open drain or push pull with appropriate termination. The JAZiO receiver uses two comparators (Comparator A and Comparator B) to compare each data signal with VTR and /VTR, respectively. Each comparator is a differential amplifier followed by a NAND gate. The outputs of both the comparators are connected to the receiver output through steering logic (consisting of two multiplexers with only one of the multiplexers being enabled at any given time). A steering logic block determines which comparator should be connected to the output as shown in Fig. 1B. The signal transfer is initiated using the comparator having full differential signal (about 0.5V) on its inputs. This comparator is connected through the multiplexer to the data output at the start of the first bit time.

As depicted in Fig. 1A, there are eight combinations of data input, VTR, and /VTR in the two consecutive bit times. In cases 1 and 6 the data input makes a differential comparison with VTR using Comparator A, in cases 2 and 5 the data input makes a differential comparison with /VTR using Comparator B, in the other four cases the data does not change. In case 1 the data and VTR both change, so after the differential comparison, Comparator A still has full differential signal at the end of the first bit time. The steering logic is essentially an exclusive OR function between data and VTR. If both of them change the same comparator remains connected to the data output through the enabled multiplexer for the next bit time. The steering logic passes the output of Comparator A to the data output and keeps the enabled multiplexer connected to the output for the second bit time. The operation is similar for case 6 relative to Comparator A and VTR and to cases 2 and 5 using Comparator B and /VTR. When the data input does not change (as in case 3), the steering logic first disables the enabled multiplexer before the differential signal between the data input and VTR disappears on Comparator A and then enables the multiplexer connecting Comparator B to the data output. Since VTR and /VTR are complementary, Comparator B has full differential signal and is driving the data output to the existing state and is ready for the second bit

time. The same VTRs are used for multiple data inputs. Up to 16 or 18 are recommended, but can be replicated for wider buses.

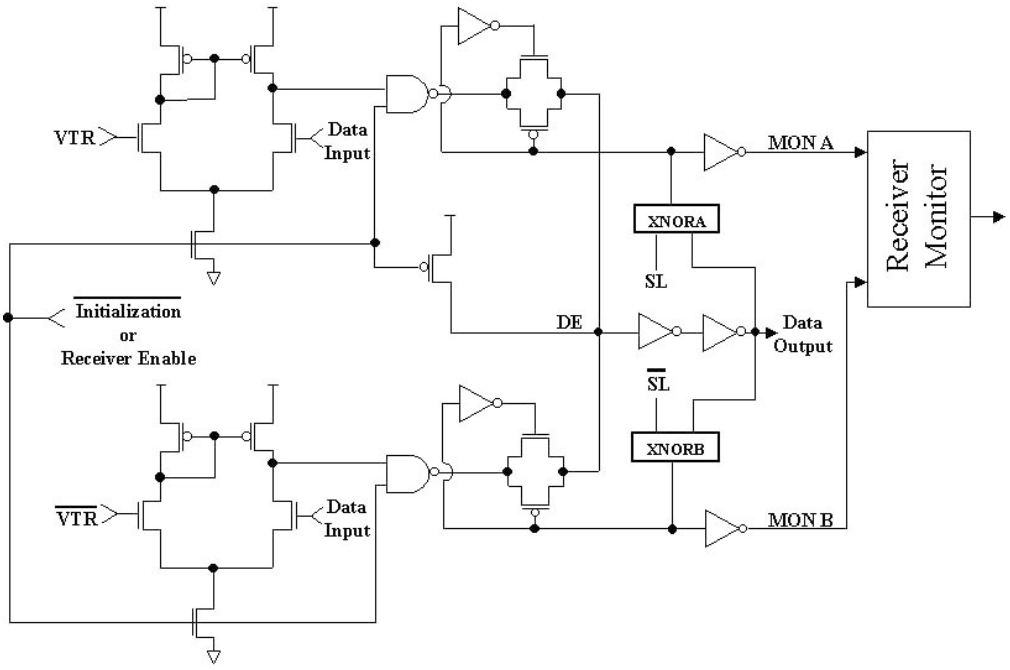


Figure 2: Transistor level receiver schematic

Figure 2 shows the receiver using N-type differential amplifiers in the comparator with very low gain to reduce receiver offset and receiver power. The multiplexer is just a simple transmission gate controlled by an XNOR gate. The XNOR gate inputs are driven by "sl" (delayed and amplified versions of the VTRs) and "sn", the receiver output. The path delay between data input to "sn" is designed to be equal to path delay between VTRs to "sl". A delayed version of the "sl" and "slb" are used to latch the data output. The additional loading on the VTRs compared to the data-in signals is about 10% if the bonding pad, input protection and the package are included. During a bit time the data input signal does not change, the previously enabled transmission gate is disabled first before the other transmission gate is enabled. The time interval between disabling the previous transmission gate and enabling the other transmission gate in the receiver is related to the amount of skew that can be tolerated between data inputs and VTRs. For example if one of the data inputs leads the VTRs by 300pS, then the "sn" changes state 300pS earlier than "sl". This will cause the XNOR to disable the transmission gate of the first comparator, which has the differential signal, and enable the transmission gate of the other comparator, which has no differential signal, temporarily creating a hazard. The XNORs are designed to break quickly and make only after the design margin for skew is satisfied. By proper sizing of devices the XNOR output is made to go high quickly, **breaking** the path from comparator to the node "DE" in Fig. 2, but go low slowly to enable the correct one later in time **making** the path from the comparator with differential signal on its input. The recommended skew band to achieve 2 gigabits/sec signal rates is shown in Fig.3. Skew margin in any implementation is dependent upon data transition time, VTR transition time and signal swing.

Assumptions:

- VTR transition time: 80% of Bit time ; Data Transition is faster

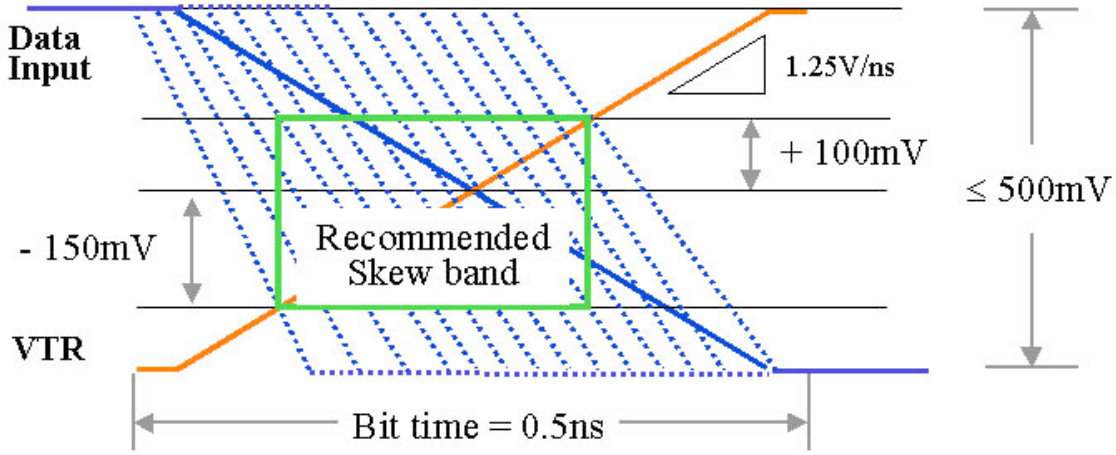


Figure 3: Data skew tolerance

The recommended skew tolerance band is indicated by the green rectangle, which is >40% of the bit time. VTRs are adjusted to be later than the data signals, as much as possible, for ease of latching and improved margins. Some skew of the data inputs beyond VTR can be tolerated. Fig. 4 depicts a simulation with -125ps (data later than VTR) and 1.66 gigabit/sec data rate. This example demonstrates a "Break-And-Remake" situation in which the data signal leads the VTR by so much that it causes an erroneous break of the path from comparator to node "DE" in Fig. 2. However, no make of the path from the other comparator occurs due to the slow fall time of the XNOR output. Correct data is stored on node DE momentarily until the XNOR recovers and remakes the path from the original comparator.

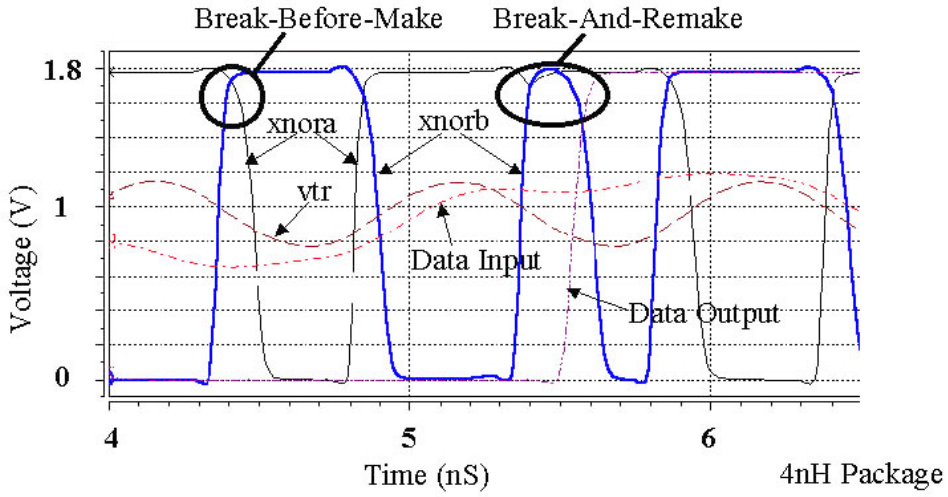
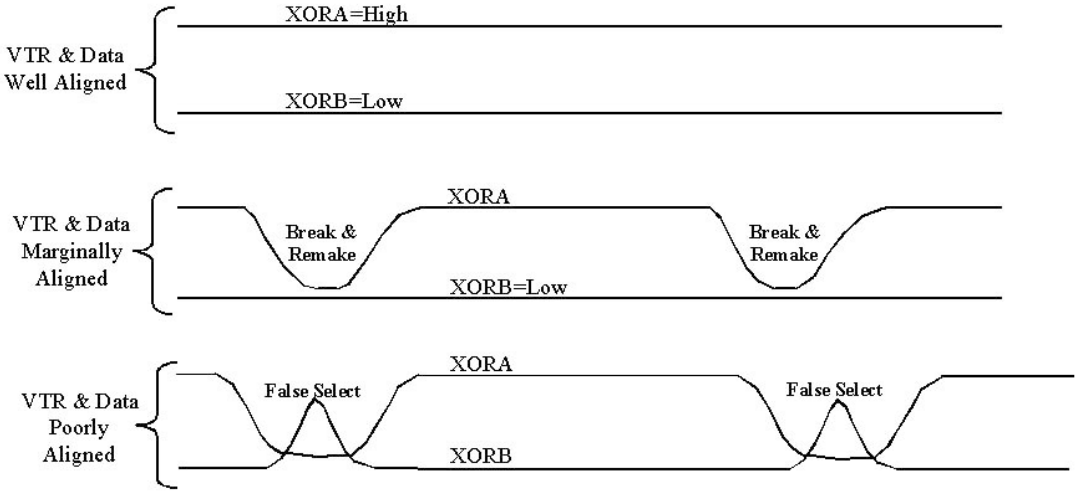


Figure 4: Data skew simulation showing XNOR handoff

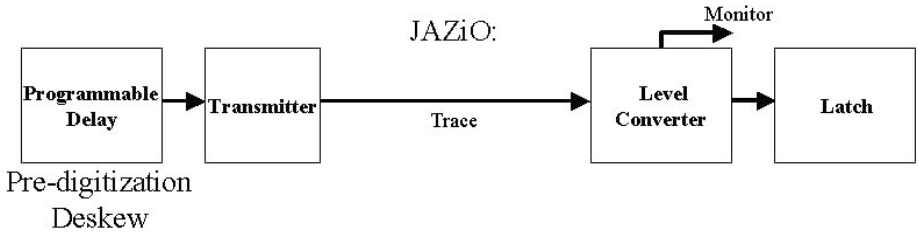
DESKEWING METHODOLOGY AND HIGH SPEED TEST MODE: The alignment of each data signal with VTRs is monitored using the receiver monitor as shown in Fig. 2. The receiver monitor is a set-reset latch, which measures transitions occurring at XNORA and XNORB with an alternating data pattern on the data signal inputs. By driving the VTRs and each data signal, which is being monitored with an alternating data pattern at the desired operating frequency, the alignment of that data signal with VTRs is monitored. If they are well aligned then MONA and MONB will have no

transition as shown on top of Fig. 5A. If the data and VTRs are marginally aligned, then we have the "Break-And-Remake" situation as shown in the middle of the Fig. 5A. If the data and VTRs are poorly aligned then both the monitors MONA and MONB will have transitions. By having programmable delays in each data driver and using the monitors to feedback the alignment information each bit can be deskewed individually to improve the data rate. This is shown in Fig. 5B, where the signal is adjusted at the source, before it is amplified or it reaches a full CMOS level. We call this Pre-digitization Deskew, as the small swing signal is adjusted in time to achieve better alignment with VTRs. This alignment technique is unique to JAZiO as the other signal switching techniques use a voltage reference (fixed for Pseudo-differential or complimentary for full differential). All previous deskewing methods were post digitization and were generally related to latching the correct data making them difficult to distinguish between level conversion marginality and signal skew. This alignment monitoring scheme can be done at power up and/or repeated whenever it is desirable in the presence of significant drift.

The receiver monitors are also used for testing the alignment of each bit with VTRs with the other bits acting as noise sources over thousands of cycles at the operating frequency. This is shown in Fig. 6. If the alignment is good then the latching and level conversion will have good margin, but bad alignment will produce possible failures. The Preamble allows the device to enter the test mode with alternating data on the data signal pin under test. All the other data signals will have various patterns to generate noise like coupling from adjacent signals, power supply noise from all the other signals transition together to the opposite levels every bit time. The monitor outputs are read back on the data pin under test when the /read signal going low as shown in Fig. 6. By having programmable delay in each data signal driver and VTRs these test can be repeated for various relative positions of data and VTRs to determine the margins and pattern sensitivities of the chip to chip connection including package, board etc at the operating frequency. This is a powerful tool to determine the early signatures during prototyping for various pin placements, package related and board related variations on the data rate and robustness of the chip to chip interface.



A) Monitor Waveforms with Alternating Data Pattern



B) Method of Monitoring and Adjusting Skew

Figure 5: Monitoring and deskewing technique

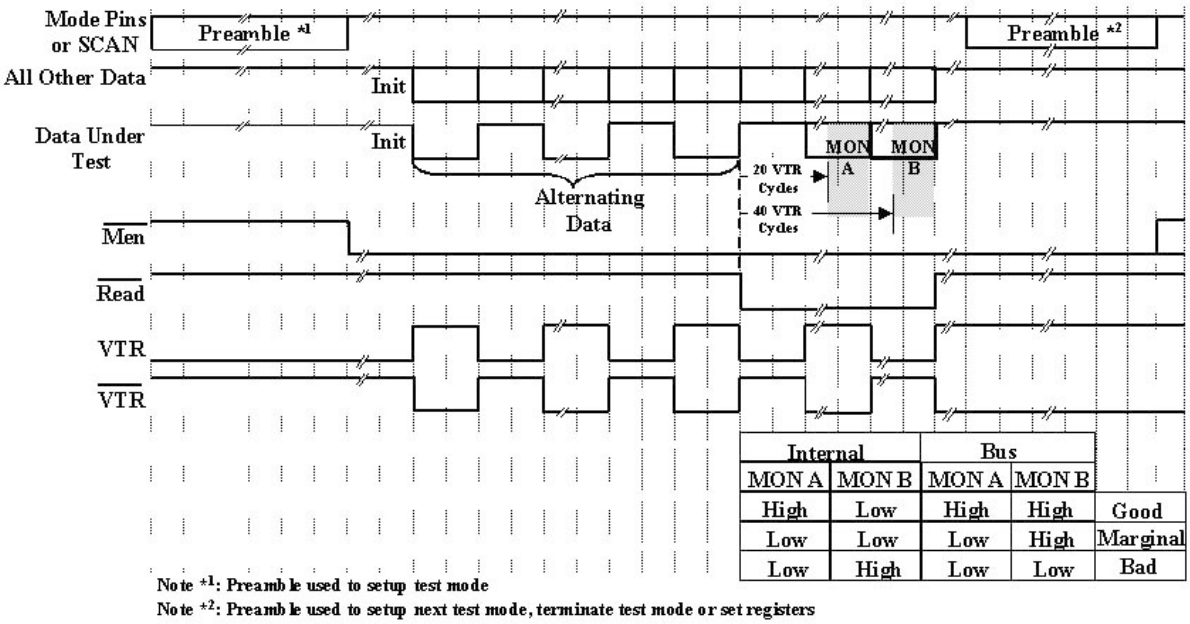
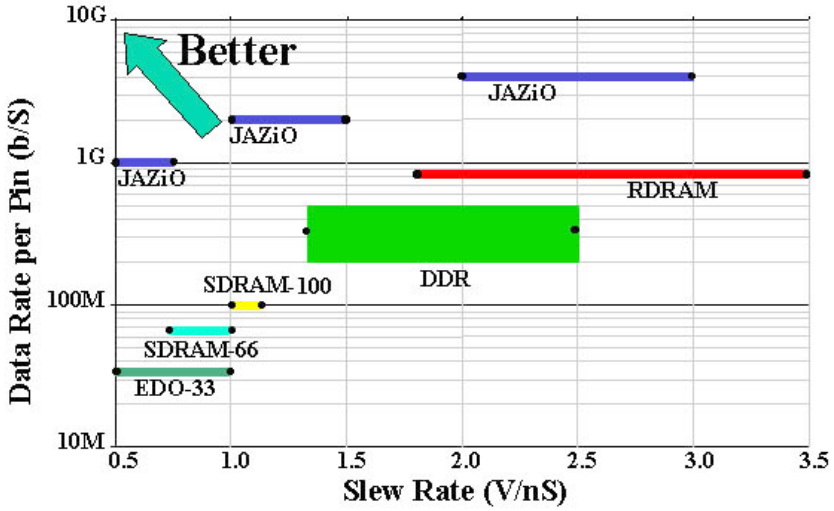


Figure 6: Single bit test mode timing diagram

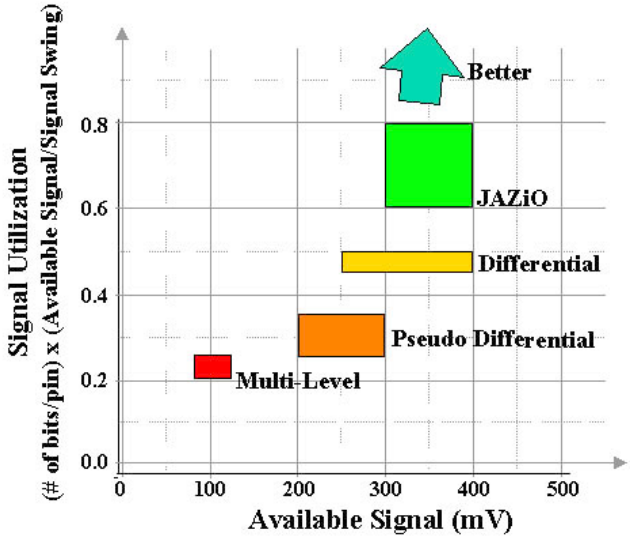
JAZiO PERFORMANCE AND COMPARISON: The JAZiO receiver uses transition detection instead of conventional voltage level detection in pseudo-differential. The differential amplifier band where the signal is detected is also about half the conventional level detection scheme using a fixed VREF. This allows better optimization of the differential amplifier especially as the power supply scales. The reduction of swing in the JAZiO scheme will additionally reduce power by shifting towards lower termination voltage. During signal amplification, the signal and the VTRs are moving in opposite directions, allowing faster operation in the differential amplifier compared to fixed VREF type implementation. Since the signal is detected during transition, there is no set-up or hold time required at the peak levels, and therefore the receiver can filter out all high-frequency noise components above the maximum operating frequency by using the input protection resistance (part of ESD) which is usually around 200Ω. The RC low-pass filter, after the bonding pad, rejects high-frequency noise allowing a smoother exponential and attenuated signal to be present at the receiver inputs. This allows lower cost (higher inductance) packages to operate at higher data rates compared to conventional pseudo-differential signal switching.

The noise sources proportional to the signal swing, (i.e. cross talk, inter-symbol-interference, signal return noise and power supply noise) are reduced by reducing the signal swing from 0.8V to 0.5V. The signal return and cross talk noise are further reduced by slowing down the transition time from 33% to 80% of the data rate. The noise sources that are independent of the signal swing, (i.e. receiver offsets) are reduced by using lower gain differential amplifiers. In figure 7A there is a comparison of JAZiO slew rate versus different DRAM technologies, this plot emphasizes the slew rate advantage of JAZiO, which can operate at 1GHz at similar slew rates as EDO-33MHz.

The reference noise commonly confronted in a fixed V_{REF} system is also eliminated as the JAZiO reference (VTRs) are real time; they have similar impedance as the signals, use the same power supplies and are subject to the same path as the signals. Any noise due to simultaneous switching of the outputs delays the VTR and signal crossing since they use the same power supplies, effectively compensating for ground bounce. The operation of JAZiO is self aligned, the data (both inputs and outputs) and VTRs shift the steering logic, change/no-change time gap and latching window in real time relative to V_{CC}, temperature and manufacturing variations resulting in a robust operation at higher frequency. The clock used for latching at the receiver of conventional system is usually based on a PLL/DLL, which is a time average of the recent supply and noise conditions and does not react instantaneously to power supply, noise and temperature. The operation of JAZiO is in real time and common mode with power supply, temperature and manufacturing variations.



A) Data versus slew rate comparison



B) Signal utilization versus available signal

Figure 7: Performance comparison between JAZiO and other signaling technologies

The minimum available signal is an important parameter due to various noise sources, high frequency signal attenuation with distance and manufacturing yields due to receiver sensitivity and offsets. It is desirable to have the smallest swing on a single pin, but still have sufficient signal for reliable sensing and low cost manufacturing. A way to define signal switching efficiency is:

Signal Switching Efficiency = (Number of Bits per Pin) x (Minimum Available Signal / Signal Swing)

Various signal switching methodologies have been plotted in figure 7B. Multi-level signaling has very small signal compared to the signal swing limiting its use to low frequency and/or extremely close chip-to-chip connections. Differential has small swing but requires two pins per bit reducing the efficiency to about 0.5. JAZiO has 300mV to 400mV of minimum available signal out of a total of 500mV swing, making it 0.6 to 0.8 efficient. This allows JAZiO to be scaleable with higher frequency, longer distances, and manufacturing variations at low cost and low power.

APPLICATIONS: JAZiO technology is useful for a wide variety of inter-chip applications like off-chip connections of DRAMs, SRAMs, CPUs, ASICs, Controllers, etc. It is also applicable for intra-chip communication between modules of large CPUs, embedded memory bus and emerging SOC (System On Chip) modules. One brief example of 16-wide MP server shown in figure 8 will be discussed. The CPU operates at 2GHz with on-chip L1 and L2 cache. The L3 cache SRAM operates at the CPU core frequency in a MCM. There are 2 or 4 SRAMs with uni-directional address bus using JAZiO operating at half the core frequency. A 32-bit bi-directional data bus shared between two banks provides 8Gbytes/sec bandwidth to the CPU. The Front-Side-Bus (FSB) is a 64-bit bus operating at 2GHz for communication through a system controller with DRAM, other processors and peripheral devices. The DRAM operates at 1GHz data rate to keep the cost low and use existing packages, modules, connectors, etc. The inter-processor communication is a uni-directional point-to-point connection operating at 2GHz. All these inter chip connections can scale up by 2x as the processor core frequency scales up over time.

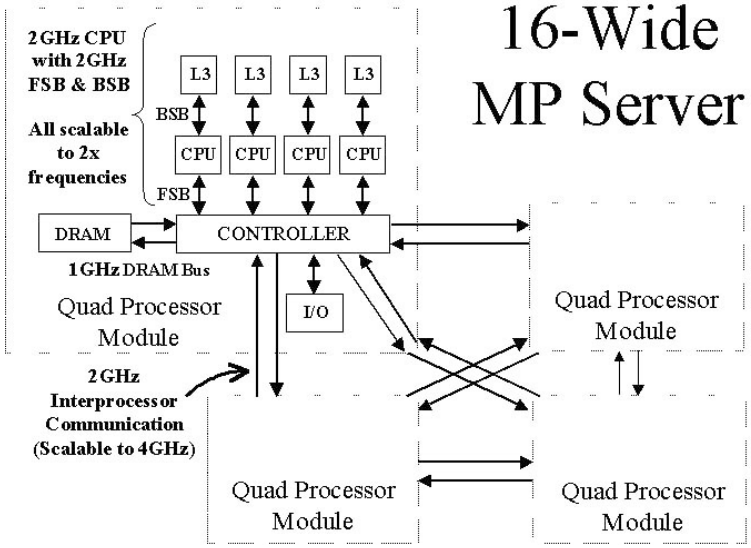


Figure 8: 16-Wide MP Server

CONCLUSION: JAZiO is a fundamentally different digital signal switching technology with the binary decision defined as a change or no-change from the previous state. Its transition detection rejects high-frequency noise at the receiver, allowing a given package, with existing ESD, to be used at a higher operating frequency (twice that of current pseudo-differential systems). The alignment monitoring scheme allows for an efficient method of deskewing data signals and testing the high speed interface. The pin bandwidth can be improved to approximately 2x differential or to approximately 5x (mainstream, low cost) conventional signal-ended switching technologies. The power reduction is about 1/2 to 1/3 of the present switching technologies. The JAZiO digital switching technology is a low-cost solution applicable to most applications. It can be used as a drop-in physical layer replacement with most of the existing protocols or can be combined with a new protocol that takes advantage of the higher pin bandwidth.

REFERENCES

[1] E. Haq, et al., "JAZiO Signal-Switching Technology: A Low-Cost Digital I/O for High-Speed Applications " IEEE MICRO, pp.72-81, January/February 2000.

[2] J. Zerbe, et al., "1.6Gb/s/pin 4-PAM Signaling and Circuits for a Multi-Drop Bus," 2000 Symposium on VLSI circuits Digest of Technical Papers, pp. 128-131, June 2000.

[3] K. Krewell. "JAZiO: Slow Edges Can Run Fast-A Novel Approach to High-Performance Bus Interfaces," in Microprocessor Report, issue 2/21/00-02, February 2000.

AUTHORS

Jim Slager is Chief Evangelist for JAZiO, Incorporated of San Jose, CA.

Bruce Barbara is President for JAZiO, Incorporated of San Jose, CA.

Ejaz Haq is Chief Technical Officer for JAZiO, Incorporated of San Jose, CA.

John Pecoraro is Executive VP for JAZiO, Incorporated of San Jose, CA.

JAZiO, Incorporated
2099 Gateway Pl STE 470
San Jose, CA 95110
Phone: (408) 487-1810
FAX: (408) 487-1814
Email: info@jazio.com