JAZiO HIGH SPEED DIGITAL I/O SIGNAL SWITCHING TECHNOLOGY

I. INTRODUCTION

JAZiO is a digital signal switching technique which uses differential sensing but requires only a single pin per signal. It is based on detecting change or no-change from the previous state instead of the traditional high or low voltage compared to a reference. JAZiO is suitable for low latency, burst mode operations for high-speed Inter-chip or Intra-chip signal transfers. Signal transfer rates of greater than two gigabits/second/pin are achievable using standard CMOS technology and existing packages at a low cost. The technology can be easily applied to DRAMs (Memory Bus), SRAMs (Back Side Bus), CPUs (Front Side Bus), Network Processors, ASICs, Intra-Chip buses etc.

II. OPERATION

A. Transmitter

The JAZiO transmitter drives a pair of alternating voltage and timing references (VTRs) coincidentally with about 16 data signals onto a bus or a receiver in a point-to-point system. The VTRs are complements of each other (VTR and /VTR) as shown in Fig. 1.

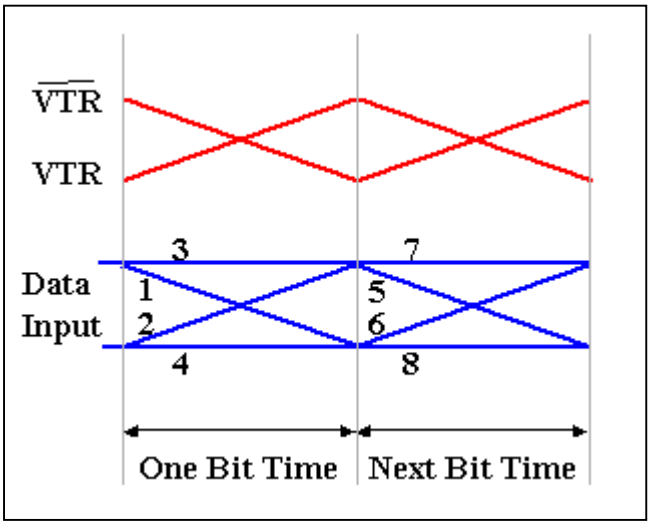

Figure 1: Data and Voltage Timing References (VTRs)

The signal swing is 0.5V or less and the transition time can be as much as a full bit time to reduce the ground bounce, cross-talk, coupling, EMI, ringing etc. The driver size is much smaller than traditional pseudo-differential drivers due to smaller swing and slower transition time. By contrast, the signal transition time, for current single ended schemes, is about 1/3 the bit-time to allow timing margins to the clock for both set-up and hold times (at the receiver) after reaching the V_{OH} or V_{OL} level. The VTR swing is about the same or less than the signals (depending on the data rate). The output driver can be an inverter or open drain (for a point-to-point connection) or an open drain or tristate (for a multi-master bus connection). The bus is initialized with all data signals starting high (the termination will pull all the signals high when they are not being actively driven as in most of the common bus configurations like GTL, HSTL, SSTL and RSL). The alternating references VTR and /VTR are initialized low and high, respectively. The VTRs transition every bit time in which the signals are transferred. Bus settling and initialization are required every time the driver source changes on the bus.

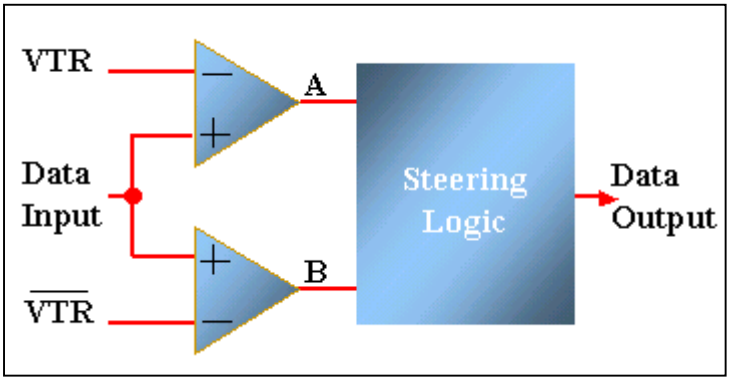

Figure 2: Simple JAZiO receiver diagram

B. Receiver

The JAZiO receiver uses two comparators (Comparator A and Comparator B) to compare each data signal with VTR and /VTR, respectively. Each comparator is a differential amplifier followed by a NAND gate. A receiver-enable signal drives the other input of the NAND gate. The outputs of both the comparators are connected to the receiver output through steering logic (consisting of two multiplexers with only one of the multiplexers being enabled at any given time). A steering logic block determines which comparator should be connected to the output as shown in Fig. 2. The signal transfer is initiated using the comparator having full differential signal (about 0.5V) on its inputs. This comparator is connected through the multiplexer to the data output at the start of the first bit time. As depicted in Fig. 1, there are eight combinations of data input, VTR, and /VTR in the two consecutive bit times. In cases 1 and 6 the data input makes a differential comparison with VTR using Comparator A, in cases 2 and 5 the data input makes a differential comparison with /VTR using Comparator B, in the other four cases the data does not change. In case 1 the data and VTR both change, so after the differential comparison, Comparator A still has full differential signal at the end of the first bit time. The steering logic (as shown in Fig. 3) is essentially an exclusive OR function between data and VTR. If both of them change the same comparator remains connected to the data output through the enabled multiplexer for the next bit time. If the data does not change then the steering logic will disconnect the data output from the previous comparator and connect the other comparator to the data output. The steering logic essentially passes the output of Comparator A to the data output and keeps the enabled multiplexer connected to the output for the second bit time. The operation is similar for case 6 relative to Comparator A and VTR and to cases 2 and 5 using Comparator B and /VTR, since all these cases have a data input

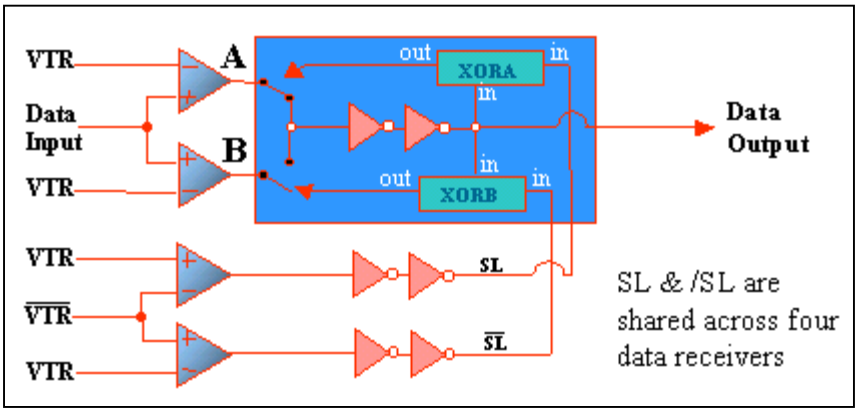

Figure 3: Steering Logic Block Diagram

change relative to the previous bit time. When the data input does not change (as in case 3), the steering logic first disables the enabled multiplexer before the differential signal between the data input and VTR disappears on Comparator A and then enables the multiplexer connecting Comparator B to the data output. Since VTR and /VTR are complementary, by

the end of the first bit time Comparator B has full differential signal and is driving the data output to the existing state and is ready for the second bit time. The same VTRs are used for multiple data inputs. Up to 16 or 18 are recommended, but can be replicated for wider buses.

C. Change/No-change Concept

In case 1 (Fig. 1) data input goes from high to low and VTR goes from low to high, each of them swinging about 0.5V. When they cross each other, the comparator (a differential amplifier followed by a NAND gate), detects the differential voltage very quickly. So in this case the comparator started with full differential signal of about 0.5V with data input being higher than VTR and ended the bit time with the same difference, but VTR being higher than the data input. This operation is well defined, deterministic and fast using current CMOS technology. If the data input does NOT change, as shown in case 3 (Fig. 1), the VTR and data input become equal at a later time than they do in their crossing in case 1. There will be a finite "time gap" between when a change occurs on the output of Comparator A in case 1 and when the output of the Comparator A becomes a weak high or indeterminate in case 3. This gap is shown in Fig. 4. When VTR and the data input become equal, the comparator output voltage is determined by the device size ratio of the differential amplifier, manufacturing variations, overshoot, etc. The comparator can be designed such that its output is a weak high when both the inputs are high and a weak low when both the inputs are low. The time gap is primarily dependent on transition time of VTR and the level of VTR compared to the data input. If the VTR transition time is exponential and takes a longer time to reach the data input level, the time gap is increased as shown in Fig. 5. The extra loading on the VTRs following the input protection resistor compared to data input ensures that the VTRs will have a longer transition time and attenuated levels at the receiver. This increases the "time gap" between a well-defined change and an indeterminate level when both the inputs (data input and VTR) to the comparator are approaching each other in value.

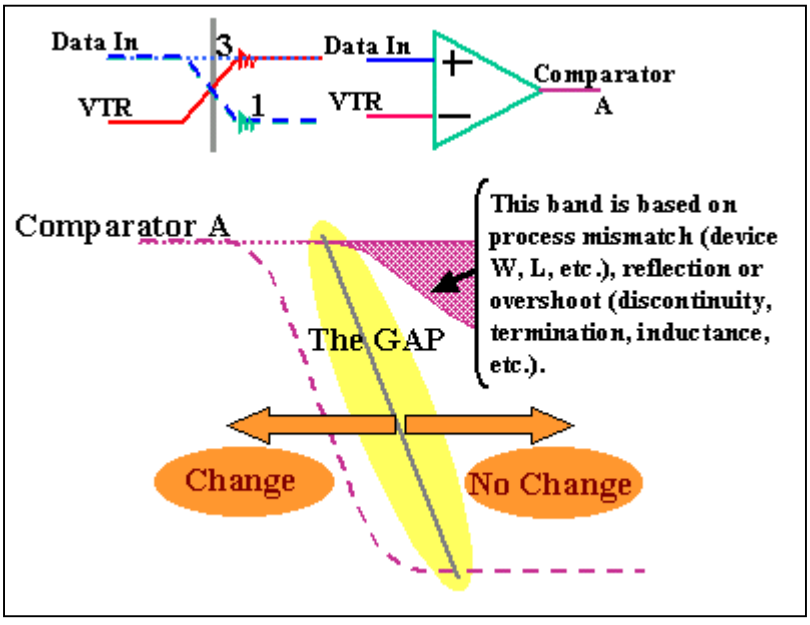

Figure 4: Change/No-change concept and gap

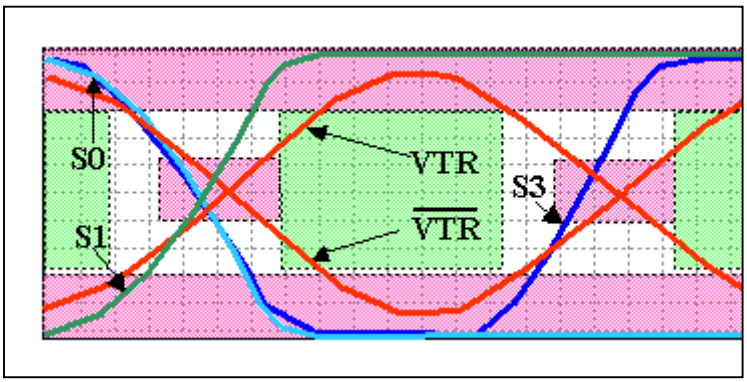

Figure 5: Change/No-change gap for VTRs having the same levels but a slower transition time than data

The steering logic is designed to allow either the change at the comparator output to pass through to the data output or to disable the already enabled multiplexer (for that comparator) in the "time gap" when no change in data input occurs. The disabling of the enabled multiplexer in the "time gap" is called the slicing time. The slicing time can be different for different signals based on data input skew, distance from VTR pads and possible adjustment of predetermined bit-to-bit skews. The increased "time gap" between change and no-change is shown as the green box with slower transitioning VTRs in Fig. 5. The VTR signals are somewhat attenuated and never reach the full swing during the bit time. The "time gap" can be designed from the transmitter by sending the VTRs at a slower slew rate than the data inputs or at the receiver by wave shaping using the additional loading of VTRs and optimizing the input protection resistor. Alternately, increased performance can be achieved by having a faster transition time on both data input and VTRs, but lower swing on the VTRs relative to the data inputs. In this case the VTRs swing is reduced using a separate power source which is approximately 100mV to 125mV lower than the data input's source. Therefore the VTRs will have approximately 300mV to 250mV swing and data inputs will have ~500mV swing as shown in Fig. 6. The 100mV to 125mV difference between data inputs and VTRs provides enough margins for the comparator to maintain the old data at its output when the data input does not change well into the next bit time, thus allowing a sufficient "time gap" to be sliced between change and no-change at much higher signal rates.

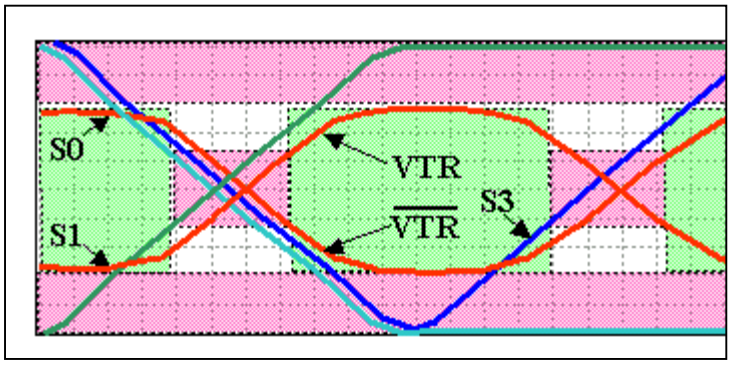

Figure 6: Change/No-change gap for VTRs having the same transition time but different levels than data

The various data-input to VTR relationships previously discussed, such as coincident, time skew and voltage skew alignment are combined into a simple concept for better understanding of the binary decision. Compared to conventional pseudo-differential signal switching where V_{OL} and V_{OH} are binary levels separated by a reference voltage V_{REF}, the

JAZiO scheme has change (which occurs early in time during signal transition) and no-change which are separated by a "time gap" with the slicing time being a reference in time similar to V_{REF} being a reference in voltage (for psuedo-differential). The decision binary in JAZiO occurs in the time domain rather than the voltage domain as in the conventional pseudo-differential scheme (this is shown in Fig. 7). The comparator with full differential signal (Comparator A) looks for the change during signal transition in the green box. If the change is not detected it adjusts to no-change by disabling the current multiplexer and enabling the other multiplexer to connect Comparator B to the data output during the yellow box time. Since the comparator is biased towards looking for change during the transition, the set-up and hold time required at the V_{OH}/V_{OL} levels for conventional signal switching are not needed in JAZiO. Higher signal rates are possible since the decision is made inside the receiver with small external voltage swings using the full bit time and no timing margins on the external pins. Even higher signal rates are possible in the future as the ability to resolve an even smaller "time gap", as the gate delays reduce with technology scaling.

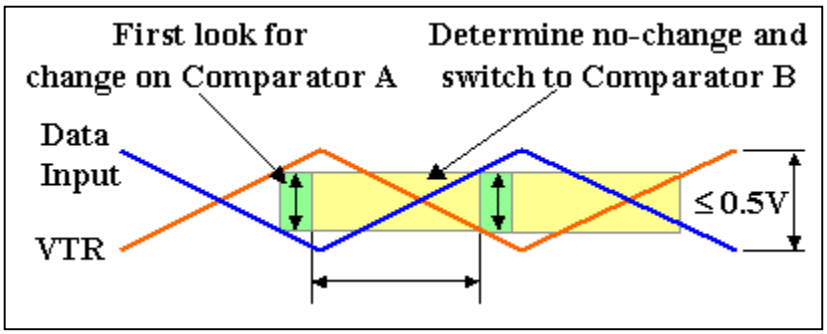

Figure 7: Time domain binary

III. Circuit Implementation

The transmitter is implemented as an open-drain N-channel driver with P-channel termination for point-to-point or an

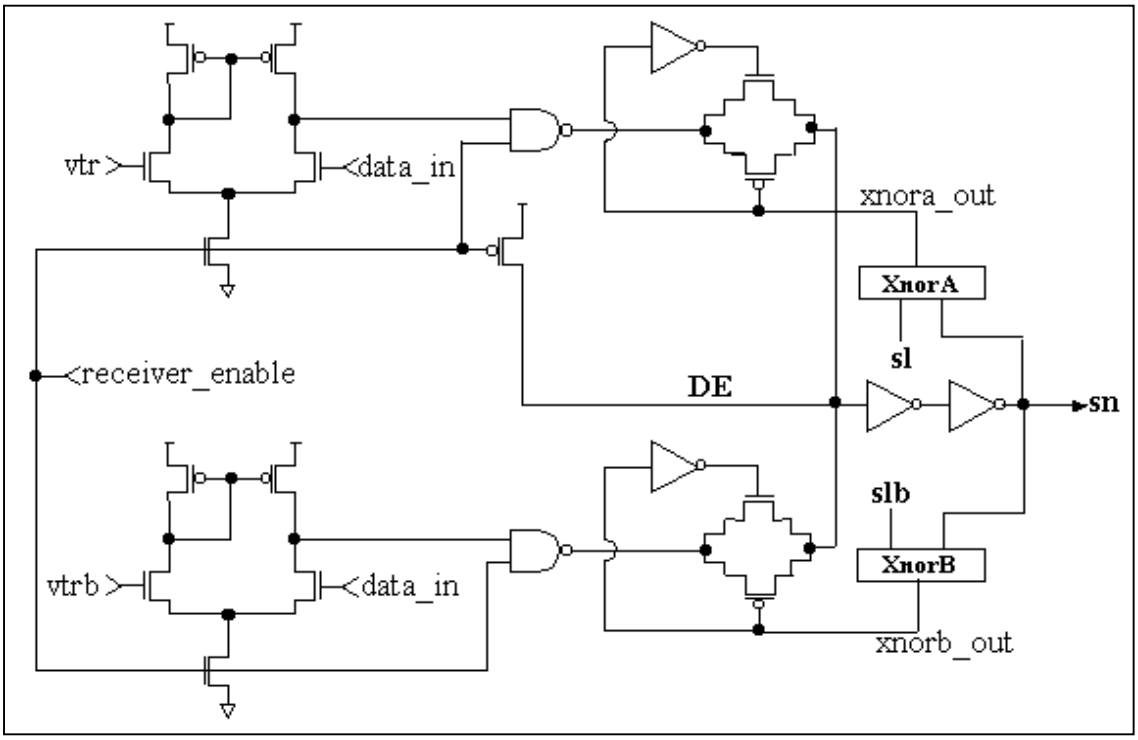

Figure 8: Transistor level receiver schematic

external resistor on both ends for a multi-drop bus. The N-channel driver is about 50µ/0.3µ in 0.18µ technology and 1.8V power supply. The termination voltage for the best speed-power product was determined to be around 1.2V for N-type differential amplifier in the receiver for this technology. The swing is designed to be about 0.5V with option for multiple slew rates on the N-channel driver from 300pS to 1nS with the target to achieve greater than 2 gigabits/second/pin in a multi-drop bus with 55Ω termination on both ends.

In Fig. 8 the receiver schematic uses N-type differential amplifiers in the comparator with very low gain (device size of 4µ/0.24µ for the N-channel and 10µ/0.24µ for the P-channel load). The ratio is based on achieving an output of the differential amplifier to be at half the power supply when there is 0.95V on both its inputs (midpoint of the 0.5V input swing). Therefore, within the normal process tolerances, the output of the comparator (differential amplifier followed by the NAND gate) will be higher than half the power supply voltage (weak high), when both the inputs to the differential amplifier are at a high level. Similarly the comparator output voltage is lower than half the power supply voltage (weak low) when both the inputs are at a low level. This increases the "time gap" between change and no-change improving operating margins. The multiplexer is just a simple transmission gate controlled by an exclusive-NOR gate. The exclusive-NOR gate inputs are driven by "sl" (delayed and amplified versions of the VTRs) and "sn", the receiver output. The path delay between data input to "sn" is designed to be equal to path delay between VTRs to "sl". During a no-change case the previously enabled transmission gate is disabled first before the other transmission gate is enabled.

A. Data to VTR skew and Latching

The time interval between disabling the previous transmission gate and enabling the other transmission gate in the receiver is related to the amount of skew that can be tolerated between data inputs and VTRs. For example if one of the data inputs leads the VTRs by 300pS, then the "sn" changes state 300pS earlier than "sl". This will cause the XNOR to disable the transmission gate of the first comparator, which has the differential signal, and enable the transmission gate of the other comparator, which has no differential signal, temporarily creating a hazard. The exclusive-NORs are designed to break quickly and make only after the design margin for skew is satisfied. The exclusive-NOR is implemented as a mux-stack type exclusive-OR followed by an inverter as shown in Fig. 9. The P-channel size is 4µ/0.2µ and N-channel is 6µ/0.2µ, so that the exclusive-OR crosses low and the inverter "C" is ratioed with P-channel device being 12µ/0.2µ and N-channel being 3µ/0.2µ. This makes the exclusive-NOR output go high quickly, **breaking** the path from comparator to the node "DE" in Fig. 8, but go low slowly to enable the correct one later in time **making** the path from the comparator with differential signal on its input. The recommended implementation can be designed for +150pS/-100pS within a group of four receivers (to be discussed later) to achieve 2 gigabits/sec signal rates. Skew margin in any implementation is

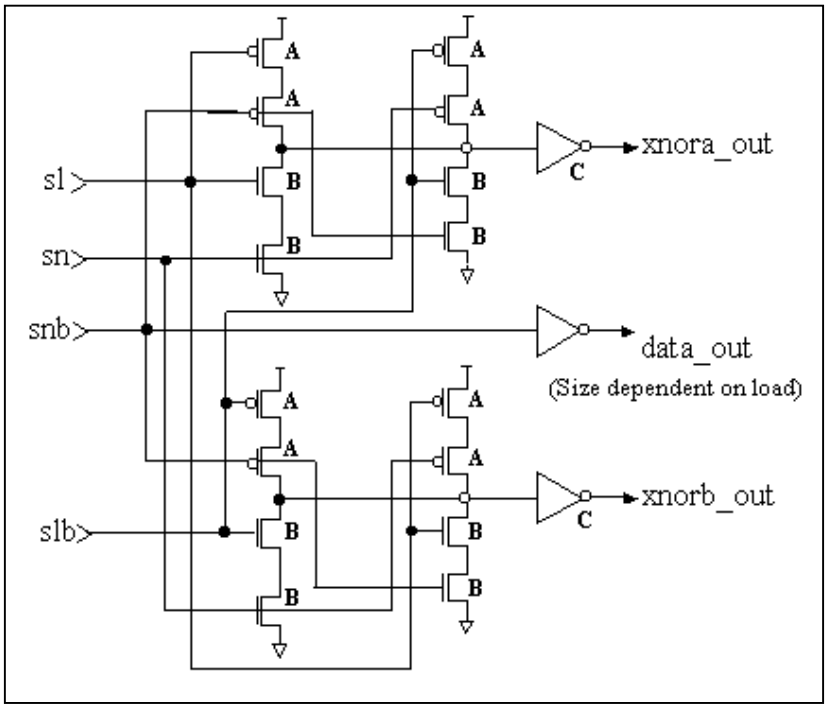

Figure 9: Exclusive-NOR schematic

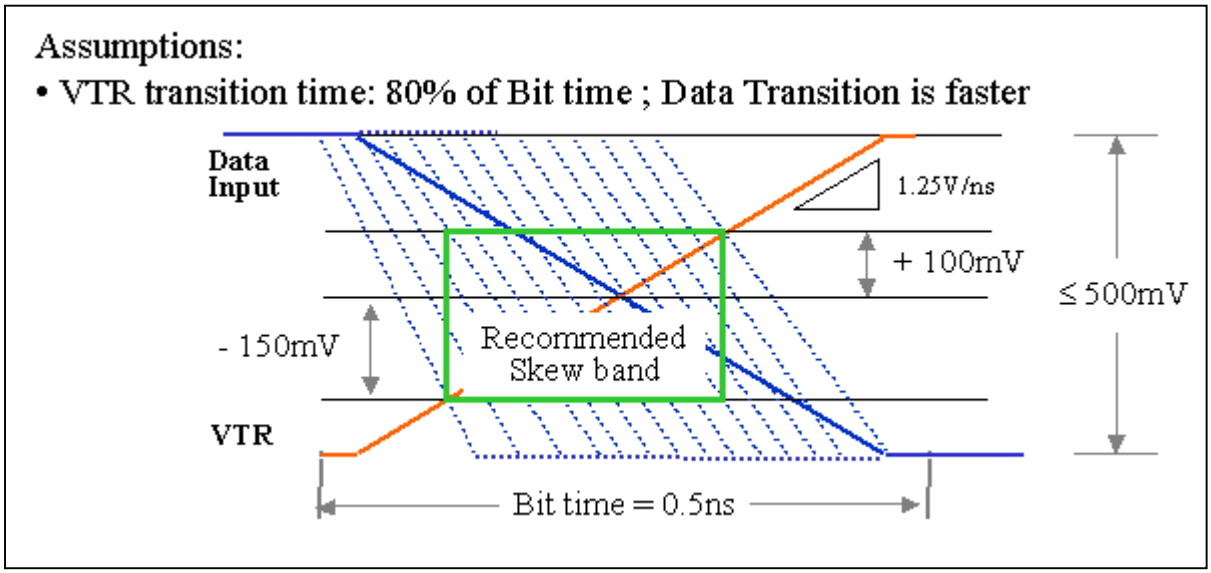

Figure 10: Data Skew Tolerance

dependent upon data transition time, VTR transition time and signal swing as shown in Fig.10. The recommended skew tolerance band is indicated by the green rectangle, which is >40% of the bit time. VTRs are adjusted to be later than the data signals, as much as possible, for ease of latching and improved margins. Some skew of the data inputs beyond VTR can be tolerated. Fig. 11 depicts a simulation with -125ps (data later than VTR) and 1.66 gigabit/sec data rate. This example demonstrates a "Break-And-Remake" situation in which the data signal leads the VTR by so much that it causes an erroneous break of the path from comparator to node "DE" in Fig. 8. However no make of the path from the other comparator occurs due to the slow fall time of the exclusive-NOR output. Correct data is stored on node DE momentarily until the exclusive-NOR recovers and remakes the path from the original comparator.

Larger skews are tolerated by programmable bit-to-bit deskewing for static or predictable skews as shown in Fig. 12. At lower signal rates, larger skews are handled by adding deglitching delays in the exclusive-NOR signal path. Since node "DE" can be floating for a short duration in every bit time, care is taken to have sufficient capacitance to avoid soft failures due to alpha particles, leakage, radiation, etc.

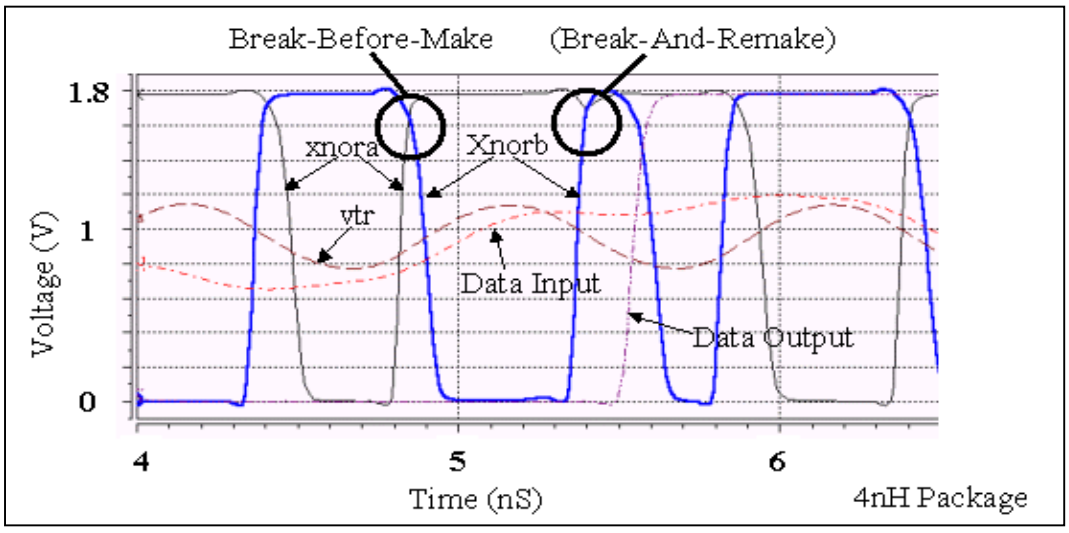

Figure 11: Data Skew simulation illustrating XNOR handoff

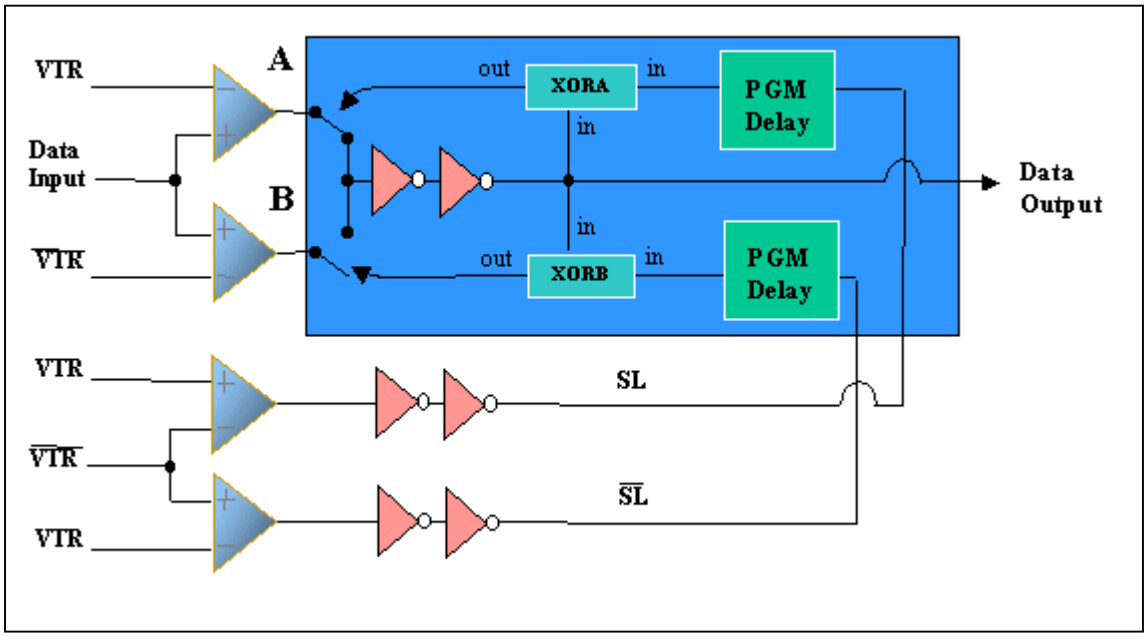

Figure 12: Steering Logic with internal SL programmable delay elements

The layout of the receiver is made symmetrical to reduce alignment variation, loading mismatches between the path from Comparator A and Comparator B to node "DE". In Fig. 13 four receivers are placed together with their own local "sl" and "slb" generator in the middle to reduce loading. Each receiver is laid out in a 100µ-wide strip to allow the data input direct access from the pad with room to put a static power or ground pin on at least one side of each data input signal.

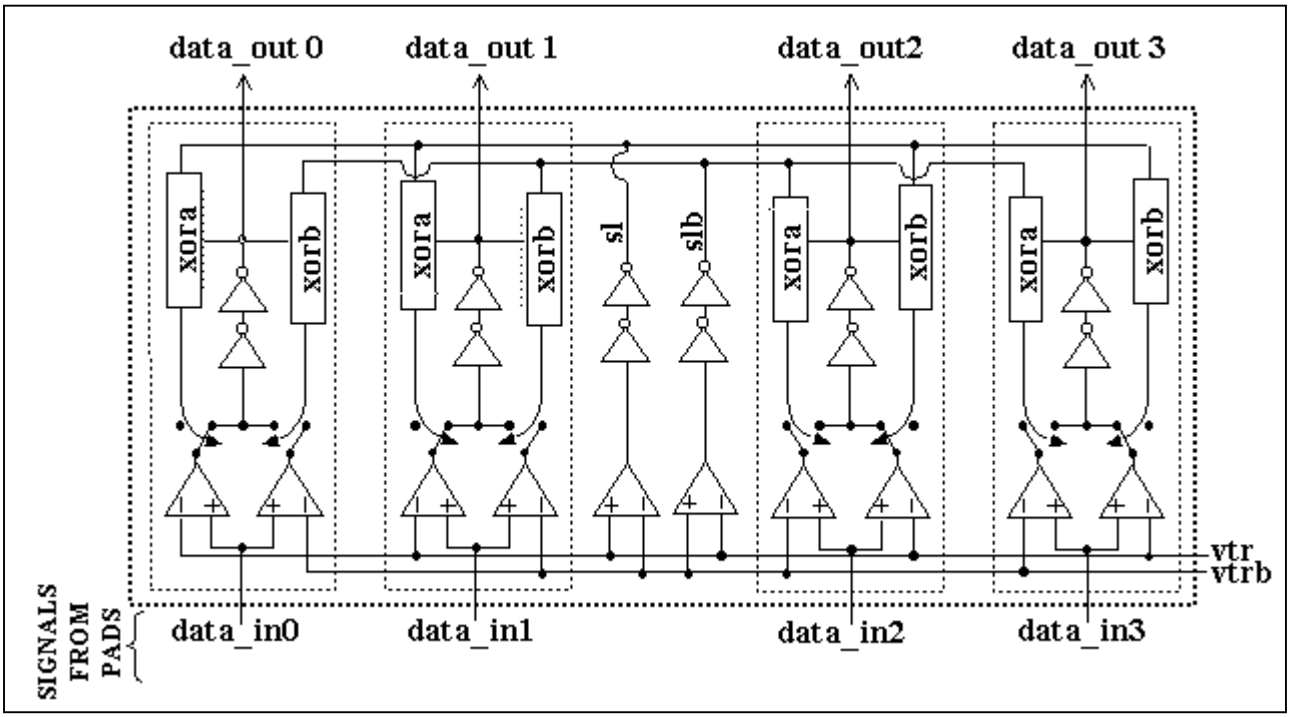

Figure 13: 4-bit receiver

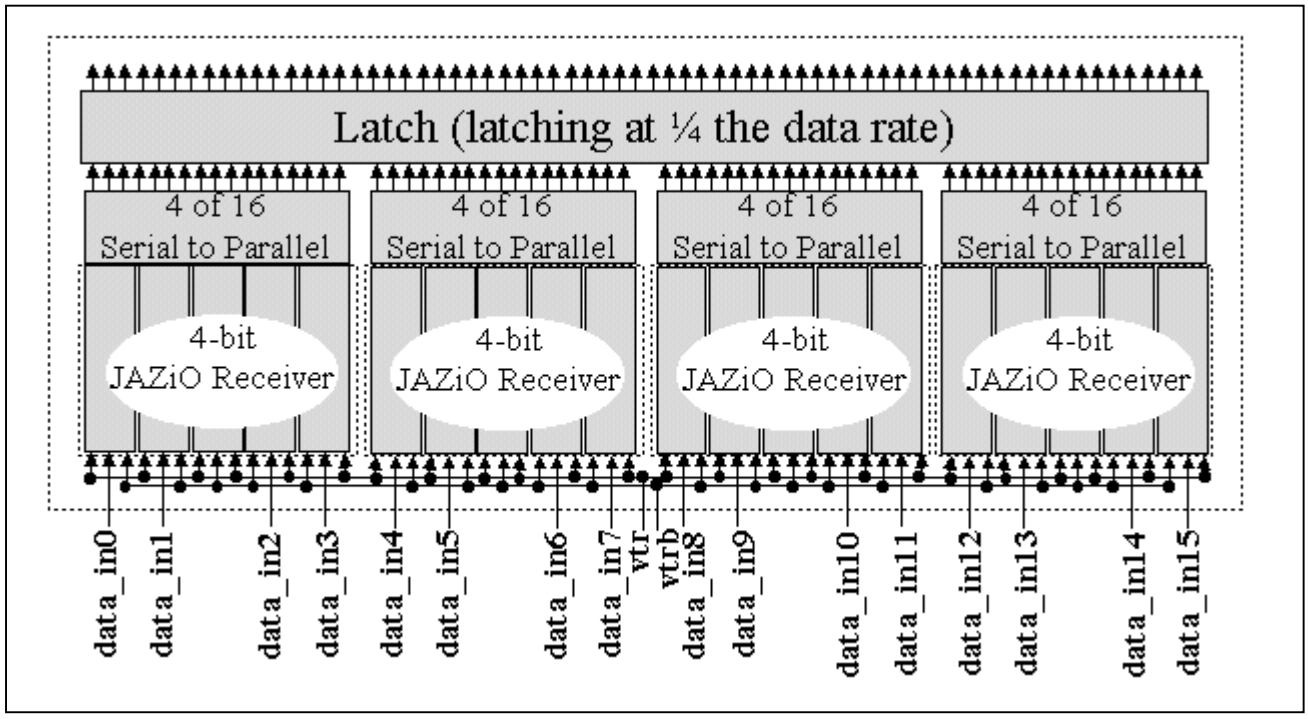

Figure 14: 16-bit receiver and latching

A delayed version of the local "sl" and "slb" are used to latch the data output for the 4 bits of a burst in the 4 of 16 serial-to-parallel converter as shown in Fig. 14. This allows better de-skewing between each group of four receivers, the following latch (used to latch the data for all serial-to-parallel converters) operates at one-fourth the signal rate. The VTR pins are routed to the middle of the sixteen receivers and are fanned out to each receiver and local "sl" generator. Since the routing of the VTRs at the receiving chip reaches data_in0 later than data_in7 (in Fig.14) the transmitting chip will drive data_in0 slightly later than data_in7, thus matching the delay of the VTRs at the receivers. The delay between the VTRs at data_in0 and data_in7 is about 10pS in the current technologies. The VTRs are isolated by ground to reduce coupling from other sources. The additional loading on the VTRs is primarily related to the metal line loading, since the gate in each comparator is 4μ/0.24μ or $1\mu^2$. The total additional capacitance on the VTRs compared to the data-in signals is about 10% if the bonding pad, input protection and the package are included.

B. Effect of Noise, Package and ESD

The JAZiO receiver uses transition detection instead of conventional peak detection (such as pseudo-differential), as shown in Fig. 15. The voltage swing required is about half the conventional single-ended scheme. The differential amplifier band where the signal is detected is also about half the conventional peak detection scheme using a fixed VREF. This allows better optimization of the differential amplifier especially as the power supply scales. The reduction of swing in the JAZiO scheme will additionally reduce power by shifting towards lower termination voltage. During signal amplification, the signal and the VTRs are moving in opposite directions, allowing faster operation in the differential amplifier compared to fixed VREF type implementation. Since the signal is detected during transition, there is no set-up or

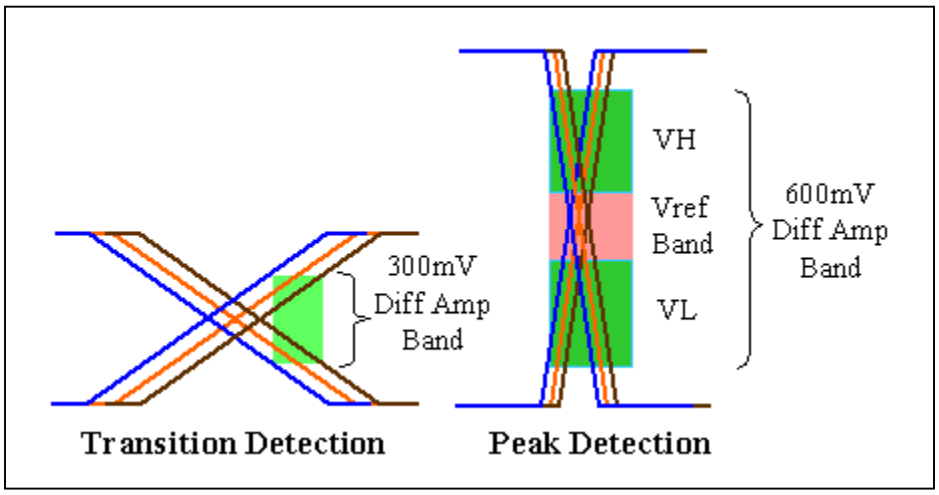

Figure 15: Peak Vs. Transition Detection

hold time required at the peak levels, and therefore the receiver can filter out all high-frequency noise components above the maximum operating frequency by using the input protection resistance (part of ESD) which is usually around 200Ω as shown in Fig.16. The simulation results with 4nH package using the model depicted in Figure 16 are shown in Figure 11 and Figure 19 at data rates of 1.66 gigabits/second/pin. The simulation results of this effect with a 2nH package are shown in Fig. 17 and Fig. 18 at signal rates of 2 gigabits/second/pin. Note: for the no-change case, the data input level at the receiver reaches a higher level (high) and lower level (low) than the VTRs. The RC low-pass filter, after the bonding pad, rejects high-frequency noise allowing a smoother exponential and attenuated signal to be present at the receiver inputs. This allows lower cost (higher inductance) packages to operate at higher data rates compared to conventional pseudo-differential signal switching.

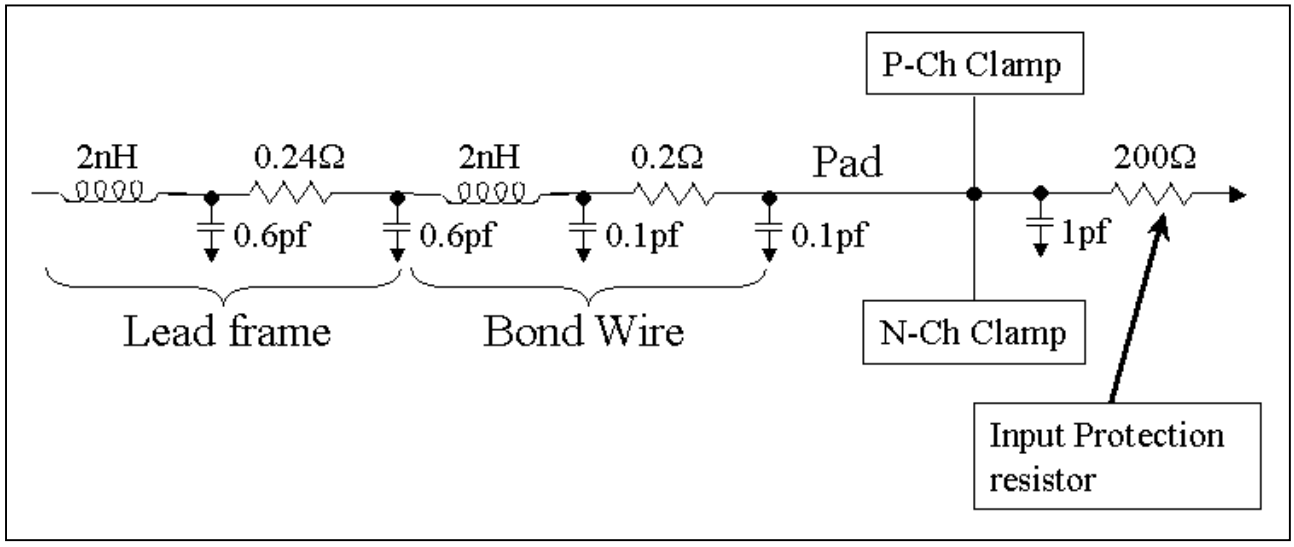

Figure 16: Package and Input protection model for 4nH package

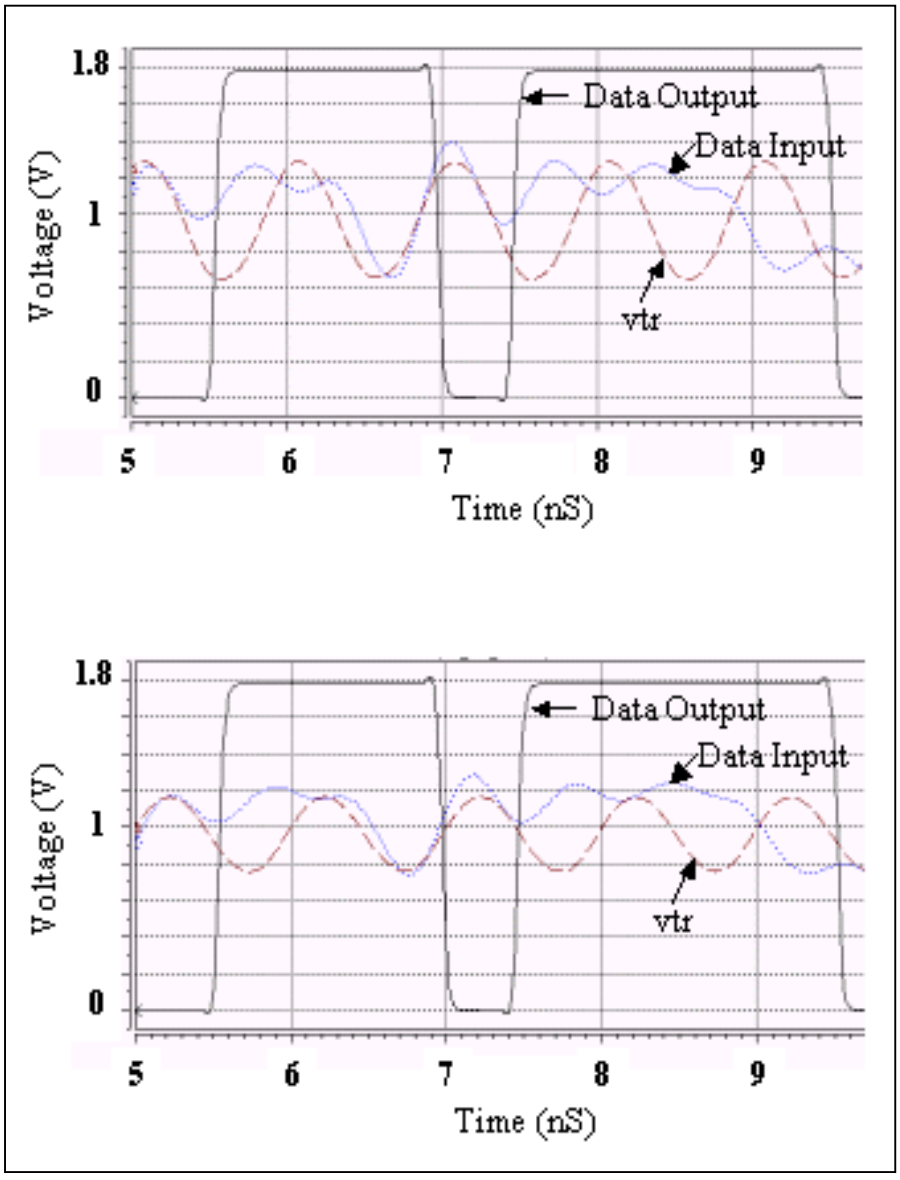

Figure 17: Upper: Simulation results at the middle of the T-line device pins; Lower: Simulation results at the receiver inputs (2Gb/s; package inductance of 2nH)

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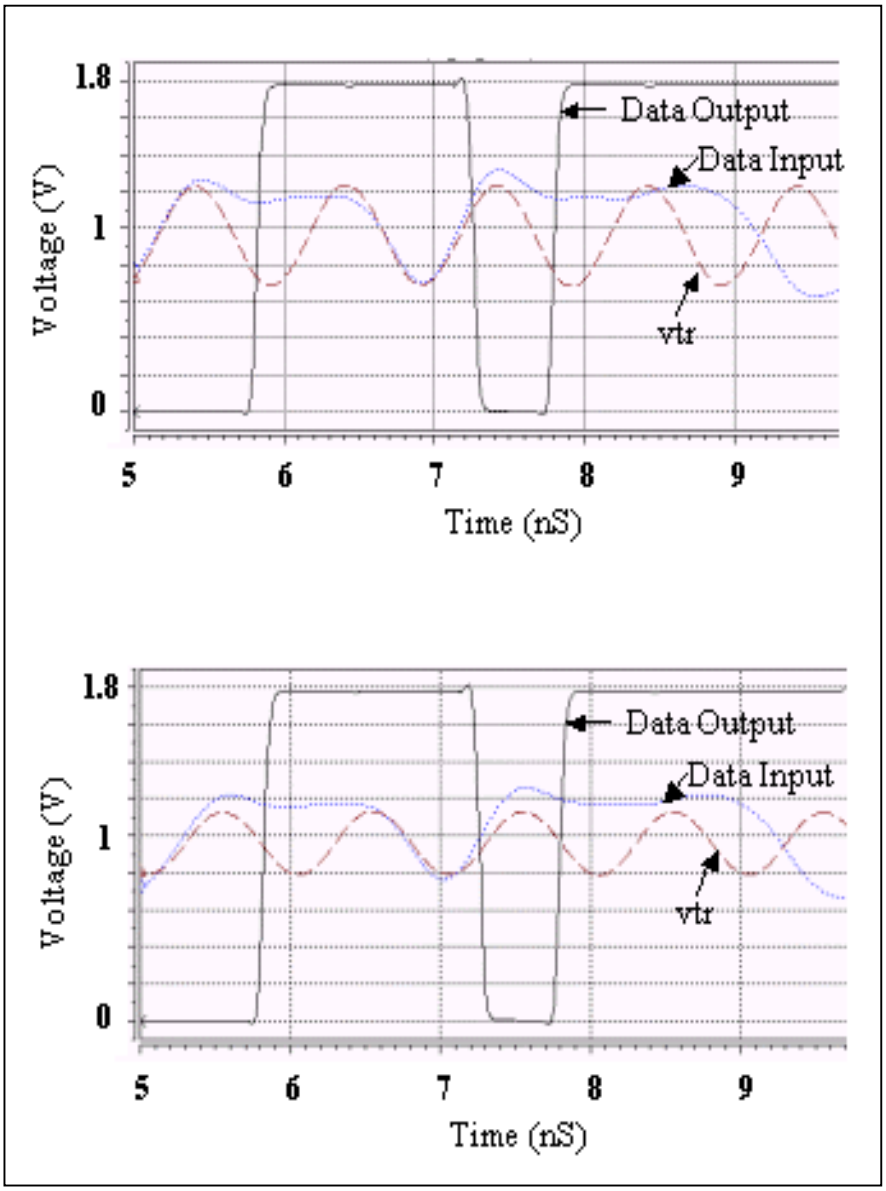

Figure 18: Upper: Simulation results at the end of the T-line device pins; Lower: Simulation results at the receiver inputs (2Gb/s; package inductance of 2nH)

In Fig. 19 a micro-Ball-Grid-Array package having 2 to 4nH can operate at 1.66 gigabits/second/pin, this could be further optimized by individually tuning the input protection resistance for different pins. Conventional peak detection schemes having set-up and hold time at the V_{OH}/V_{OL} needs to allow much higher frequency components (up to 3 times the desired

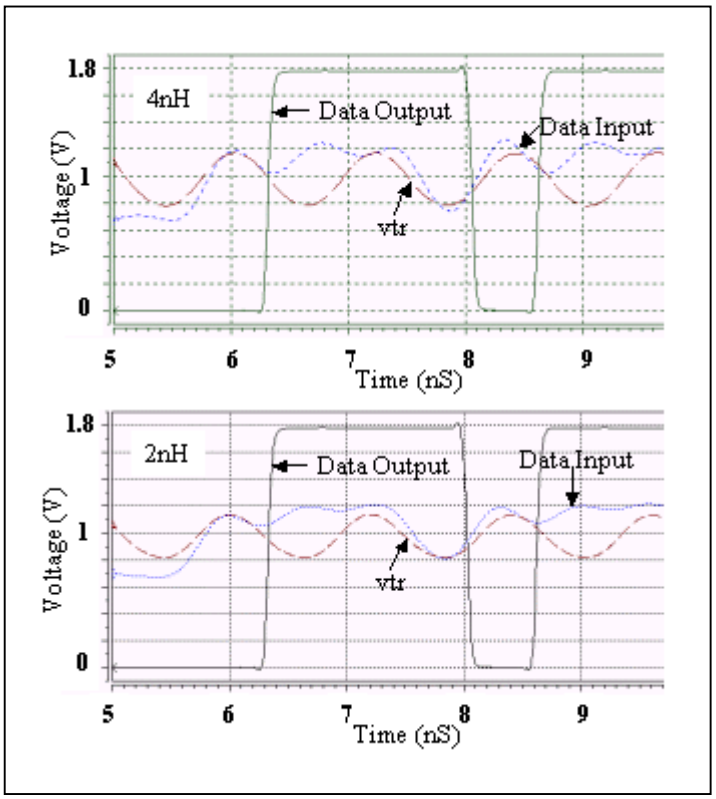

Figure 19: Simulation results at the middle of the T-line at the receiver inputs (1.66Gb/s; package inductance of 4nH and 2nH)

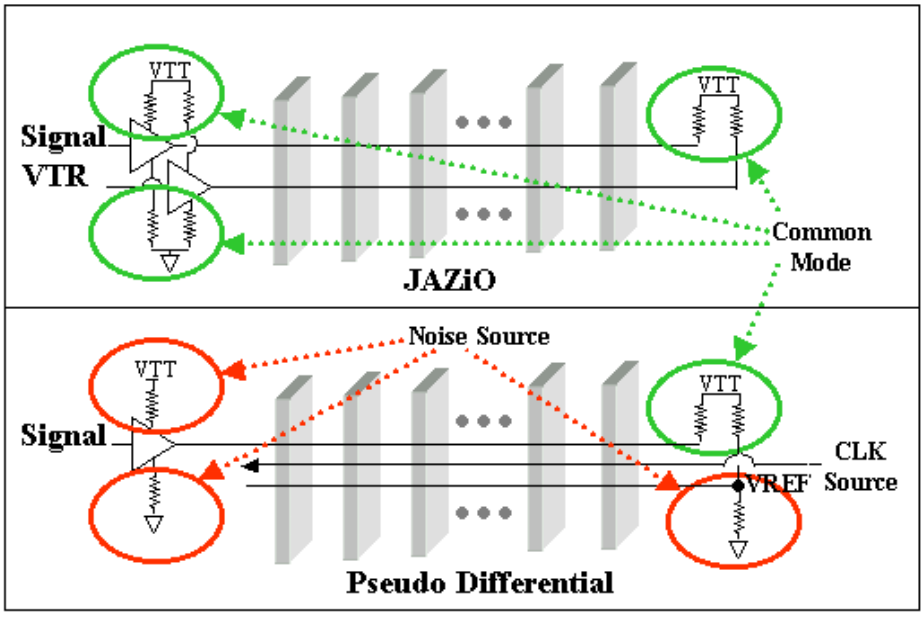

Figure 20: Noise source comparison

maximum operating frequency) to be present at the receiver to amplify and latch the signal using a synchronous clock.

The reference noise commonly confronted in a fixed V_{REF} system is also eliminated as the JAZiO reference (VTRs) are real time; they have similar impedance as the signals, use the same power supplies and are subject to the same path as the signals as illustrated in Fig. 20. Any noise due to simultaneous switching of the outputs delays the VTR and signal crossing since they use the same power supplies, effectively compensating for ground bounce. The operation of JAZiO is self aligned, the data (both inputs and outputs) and VTRs shift the steering logic, change/no-change time gap and latching window in real time relative to V_{CC}, temperature and manufacturing variations resulting in a robust operation at higher frequency. The fixed V_{REF} used in the conventional system is an average of V_{CC}, temperature, manufacturing variations, and instantaneous noise; therefore it cannot react to real-time changes occurring at the transmitter. Likewise the clock used for latching at the receiver of conventional system is usually based on a PLL/DLL, which is a time average of the recent supply and noise conditions and does not react instantaneously to power supply, noise and temperature. The operation of JAZiO is in real time and common mode with power supply, temperature and manufacturing variations.

IV. Applications

JAZiO technology is useful for a wide variety of inter-chip applications like off-chip connections of DRAMs, SRAMs, CPUs, ASICs, Controllers, etc. It is also applicable for intra-chip communication between modules of large CPUs, embedded memory bus and emerging SOC (System On Chip) modules. Two brief DRAM examples will be discussed to explain how this technology can be applied to achieve high performance at low power and low cost.

A. Low Cost DRAM Application

Fig. 21 shows a parallel DRAM system (dual channel) achieving 8 gigabytes/second with each 16-bit-wide wide DRAM device operating at 2 gigabits/second/pin. The address and control bus are shared between all the DRAMs. The unidirectional address and control bus uses its own VTR0s to receive signals. This bus can operate at the same signal rate or half the signal rate depending on the burst length of data and protocol. The VTR0s are essentially a source synchronous

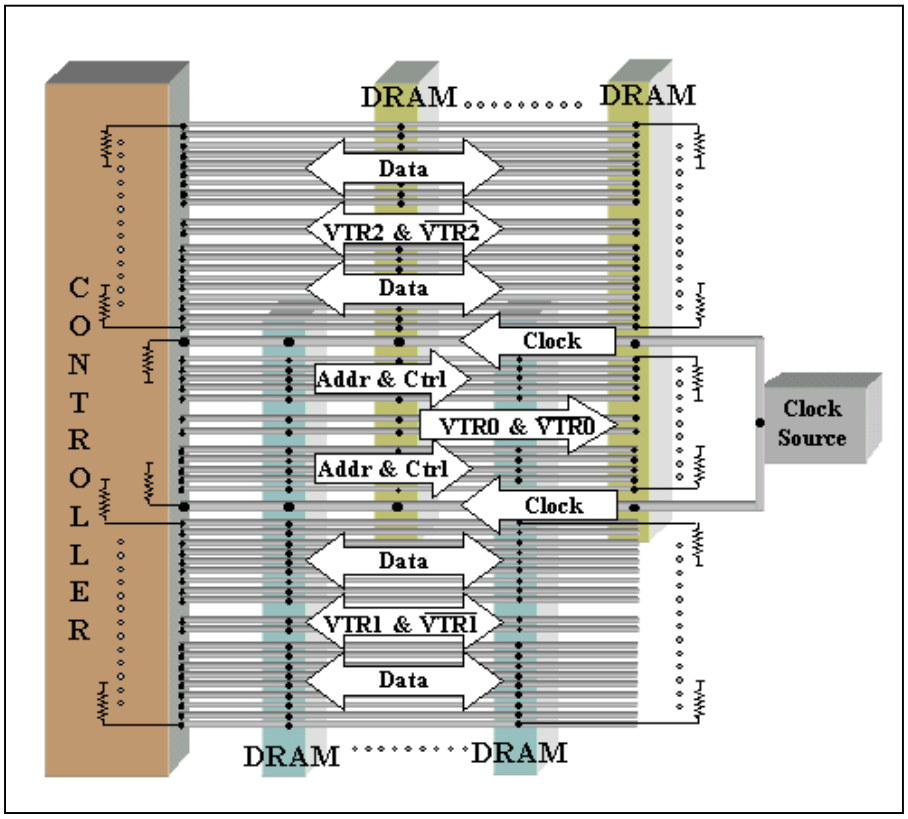

Figure 21: Low cost DRAM sub-system

clock from the controller. When all the control signals are high, it is interpreted as a NOP by the DRAM. The bi-directional VTR1s & VTR2s are used by the DRAMs to send or receive data. The DRAM does not require any PLL/DLL thus reducing cost and power. Every time the data source changes the receiver needs to be initialized and the bus needs to settle down. This costs two bit times or one cycle, reducing the bus efficiency, which is common for most of the upcoming DRAMs. The advantage of this system apart from higher data rates is the address and control signal bus can be shared in dual channel configuration (unlike Direct RDRAM dual channel, which requires separate address and control signals for each channel). This shared address and control bus operates at the same signal rate as data, requiring fewer pins and providing better data bus utilization compared to Double-Data-Rate DRAM.

B. Low Power DRAM Application

Fig. 22 shows a low power hand held system with a SOC talking to an external DRAM. The address, control and data (writing to DRAM) are shared on a 17-pin or 33-pin unidirectional bus, depending on the read to write ratio. The extra pin determines whether the SOC is sending data or addresses. The DRAM read data are on a separate 32-pin unidirectional bus. The DRAM has multiple internal banks to allow writing in one bank while reading another. Extra buffers in both SOC and DRAM allow temporary data storage to avoid or minimize read/write to the same bank. Since the connection is point-to-point and unidirectional, it can operate without a low impedance external termination, instead, using approximately a 90Ω P-Channel pull-up to limit voltage swing, with slow transition times (using the full bit time). The address and control can be sent in one cycle for long burst reads of 64 bytes reducing power in the DRAM array. The interface power in this system for 3 gigabits/second/pin data rate is approximately 7 milliwatts/pin. The small voltage swing and slow transition times reduce the EMI, which is an important consideration for consumer applications.

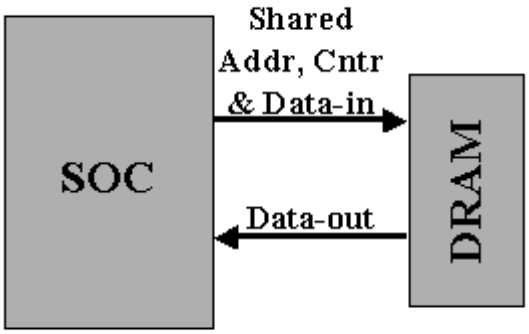

Figure 22: Low power DRAM application

V. CONCLUSION

JAZiO is a fundamentally different digital signal switching technology with the binary decision defined as a change or no-change from the previous state. Its slower edges with smaller voltage swing reduces power and noise. Its transition detection rejects high-frequency noise at the receiver, allowing a given package to be used at a higher operating frequency (twice that of current pseudo-differential systems). The pin bandwidth can be improved to approximately 2x (bleeding edge, LVDS) to approximately 5x (mainstream, low cost) of the conventional signal-switching technologies. The power reduction is about 1/2 to 1/3 of the present pseudo-differential switching technology. Since JAZiO technology does not rely on PLL / DLL, single cycle activation further reduces system power as compared to other high speed technologies. JAZiO can use existing ESD structures due to its slower edge rates, thereby improving reliability. The JAZiO digital switching technology is a low-cost solution applicable to most applications. It can be used as a drop-in physical layer replacement with most of the existing protocols or can be combined with a new protocol which takes advantage of the higher pin bandwidth.

REFERENCES

[1] K. Krewell. "JAZiO: Slow Edges Can Run Fast-A Novel Approach to High-Performance Bus Interfaces," in Microprocessor Report, issue 2/21/00-02, February 2000.

[2] B. Lau, et al., "A 2.6GB/s Multi-Purpose Chip-to-Chip Interface," ISSCC Digest of Technical Papers, pp. 162-163, February 1998.

[3] C. Kim, et al., "A 640MB/s Bi-Directional Data Strobed, Double-Data-Rate SDRAM with a 40mW DLL Circuit for a 256MB Memory System," ISSCC Digest of Technical Papers, pp. 158-159, February 1998.

[4] H. Tamura, et al., "PRD-Based Global-Mean-Time Signaling for High-Speed Chip-to-Chip Communications," ISSCC Digest of Technical Papers, pp. 164-165, February 1998.